DIGITAL SIGNAL PROCESSING

DIGITAL THEORY

ANALOG: A SYSTEM CAPABLE OF PRODUCING AN OUTPUT THAT IS CONTINUOUSLY VARIABLE

DIGITAL - A SYSTEM THAT PRODUCES AN OUTPUT OF TWO STATES ONLY.

CMOS : COMPLEMENTARY METAL OXIDE SILICON
N & P CHANNEL MOS FETs.
LOW SPEED / LOW POWER CONSUMPTION

TTL - TRANSISTOR TRANSISTOR LOGIC
HIGH SPEED

DTL - DIODE TRANSISTOR LOGIC
A COMBINATION OF TRANSISTORS AND D
IMPLEMENT THE REQUIRED FUNCTION

HTL - HIGH THRESHOLD LOGIC
HIGH NOISE IMMUNITY
ESPECIALLY USEFUL IN INDUSTRIAL
CONTROL APPLICATIONS.

ECL - EMITTER COUPLED LOGIC.
VERY SHORT GATE PROPAGATION
DELAY TIME.

TORS AND DIODES TO

FUNCTION

DUSTRIAL

AGATION

LOGIC → COMBINATIONAL LOGIC – OUTPUT CAN BE PREDICTED AT ANY TIME PROVIDED THAT INPUTS ARE KNOWN

→ SEQUENTIAL LOGIC – TIME + MEMORY IN TO SYSTEM

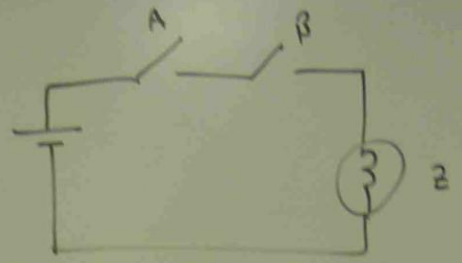
SYNCHRONOUS LOGIC – MASTER (CLOCK – SQUARE WAVE GENERATOR)

– PROVIDE REGULAR TIMING (OR) CLOCKING PULSES.

ASYNCHRONOUS LOGIC – EVENTS OCCUR AFTER THE P/REVIOUS EVENT IS COMPLETED.

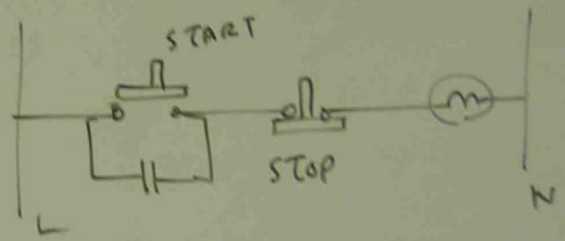
– TO SETUP CHAIN REACTION OF EVENTS.

AND GATE

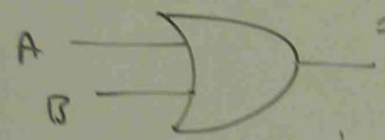


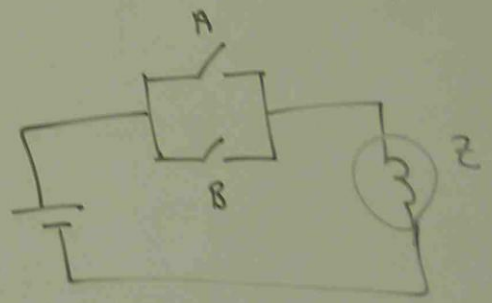
TRUTH TABLE

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1



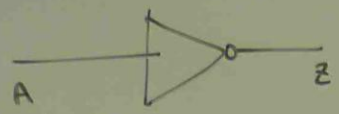
OR GATE



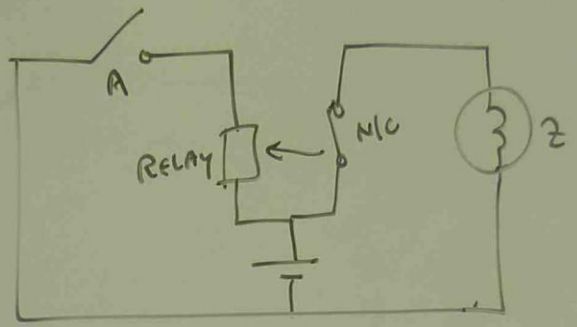


A	B	Z
1	0	1
0	1	1
1	1	1
0	0	0

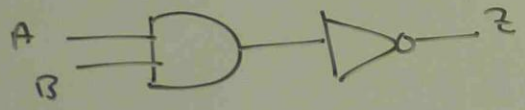
NOT GATE (INVERTER)



A	Z
0	1
1	0



NAND GATE



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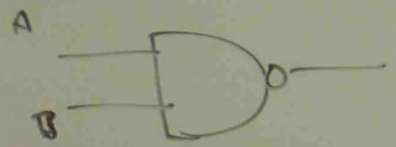
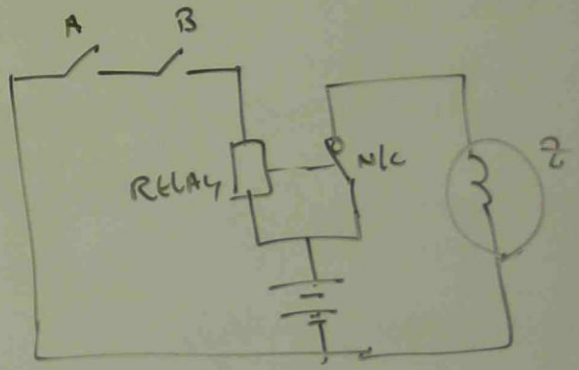
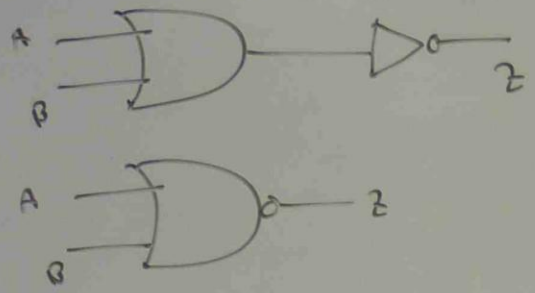


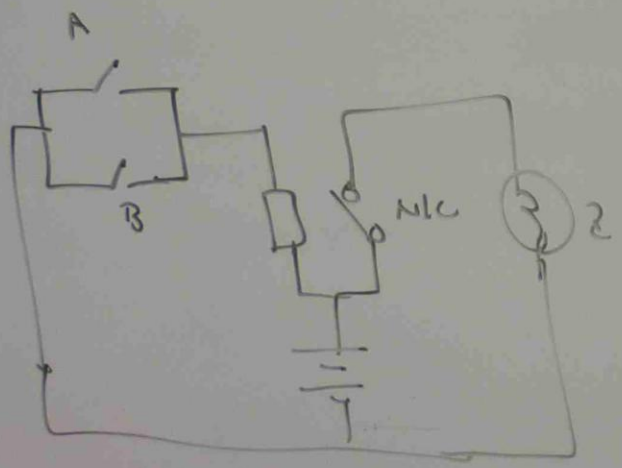
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0



NOR GATE

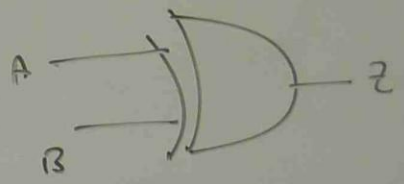


A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0



EX-OR

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0



GATE	CMOS	TTL
NOT INVERTOR	4069	7404

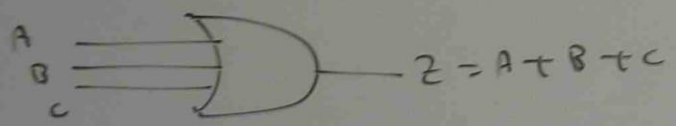
ICs

GATE TYPE	COMS	TTL
AND	4081	7408
OR	4071	7432
NAND	4011, 4023 4012, 4068	7400, 7410 7420, 7430
NOR	4001	7402
EX OR	4070	7486
EX NOR	4077	9386

BOOLEAN ALGEBRA

AND

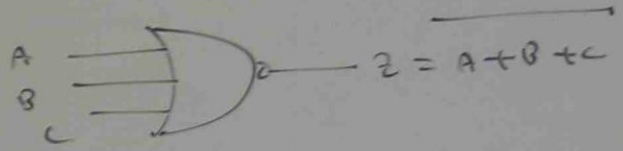
OR



NOT

NAND

NOR



BOOLEAN POSTULATES

$0 \cdot 0 = 0$

$1 + 1 = 1$

$0 + 0 = 0$

$1 \cdot 1 = 1$

$1 \cdot 0 = 0 \cdot 1 = 0$

$1 + 0 = 0 + 1$

$A + 0 = A$

$A \cdot 0 = 0$

$A + 1 = 1$

$A + A = A$

$A \cdot A = A$

$A + \overline{A} = 1$

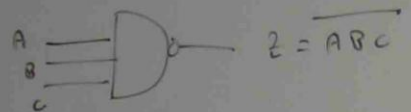
$A \cdot \overline{A} = 0$

$A + B = B + A$

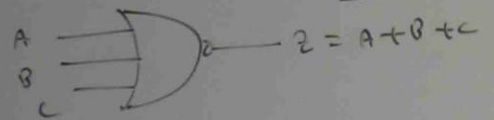
$\overline{\overline{A}} = A$

$A \cdot B = B \cdot A$

NAND



NOR



BOOLEAN POSTULATES

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$1.1 = 1$

$1.0 = 0.1 = 0$

$1+0 = 0+1 = 1$

$A+0 = A$

$A.0 = 0$

$A+1 = 1$

$A+A = A$

$A.A = A$

$A+\overline{A} = 1$

$A.\overline{A} = 0$

$A+B = B+A$

$\overline{\overline{A}} = A$

$A.B = B.A$

DEMORGAN THEOREM

$$A+B = \overline{\overline{A}.\overline{B}}$$

$$(A.B).(C+D) = \overline{(\overline{A}+\overline{B})+(\overline{C+D})}$$

EQUIVALENT

USE NAND

GATE	NAND
NOT	
AND	
OR	
NAND	
NOR	

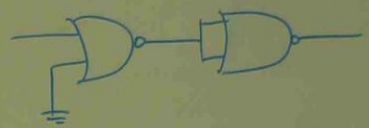
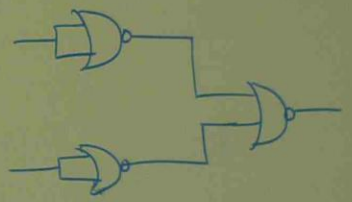
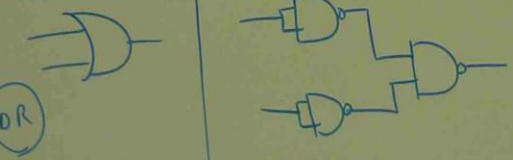
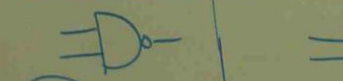
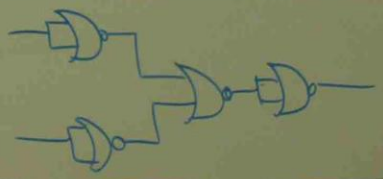
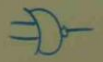
DEMORGAN THEOREM

$$A + B = \overline{\overline{A} \cdot \overline{B}}$$

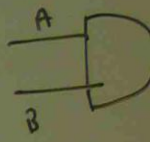
$$(A \cdot B) \cdot (C + D) = (\overline{A} + \overline{B}) + \overline{(C + D)}$$

EQUIVALENT GATES

USE NAND & NOR GATES TO GET AND, OR, NOR, EX OR NOT FUNCTIONS.

GATE	NAND EQUIVALENT	NOR EQUIVALENT
NOT		
AND		
OR		
NAND		
NOR		

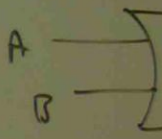
AND



TRUTH

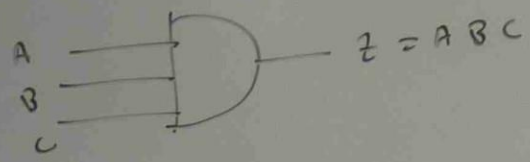
A	B
0	0
0	1
1	0
1	1

OR

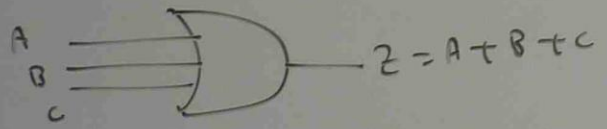


BOOLEAN ALGEBRA

AND

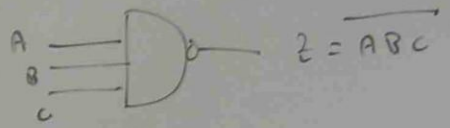


OR

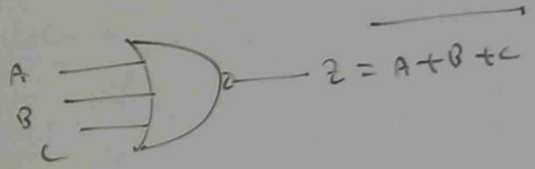


NOT

NAND



NOR



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$A+\overline{A} = 1$

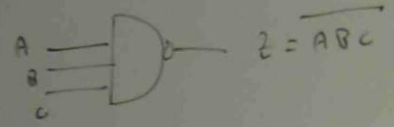
$A.\overline{A} = 0$

$A+B = B+A$

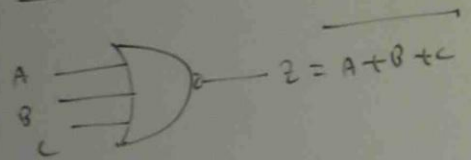
$\overline{\overline{A}} = A$

$A.B = B.A$

NAND



NOR



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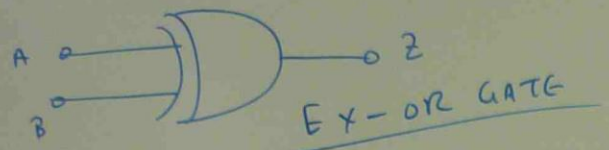
EQUIVALENT GA

USE NAND &

GATE	NAND EQUI
NOT	
AND	
OR	
NAND	
NOR	

ADDER CIRCUIT



EX-OR GATE

TRUTH TABLE

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

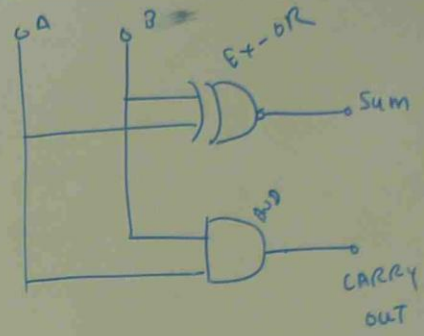
$$\begin{array}{r} 9 \\ +\ 1 \\ \hline 1\ 0 \end{array}$$

↑ CARRY

$$\begin{array}{r|l} 2 & 9 \\ \hline & 4 \end{array}$$

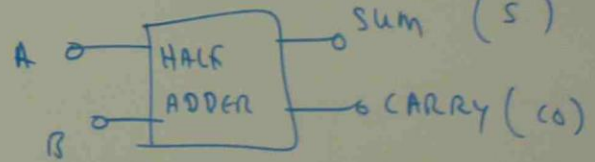
1

HALF ADDER



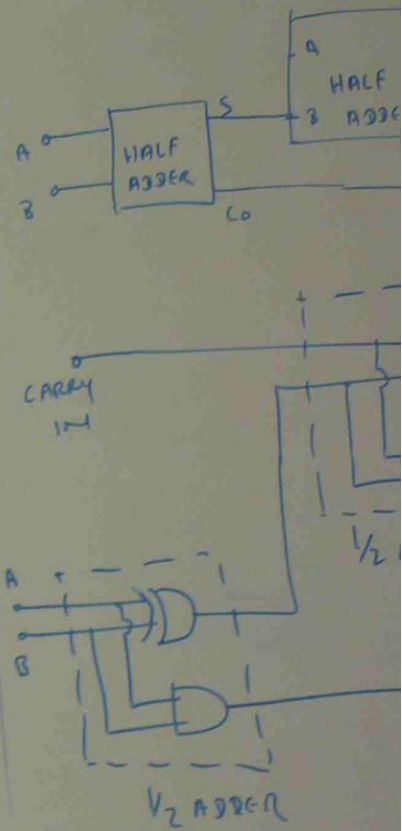
TRUTH TABLE

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

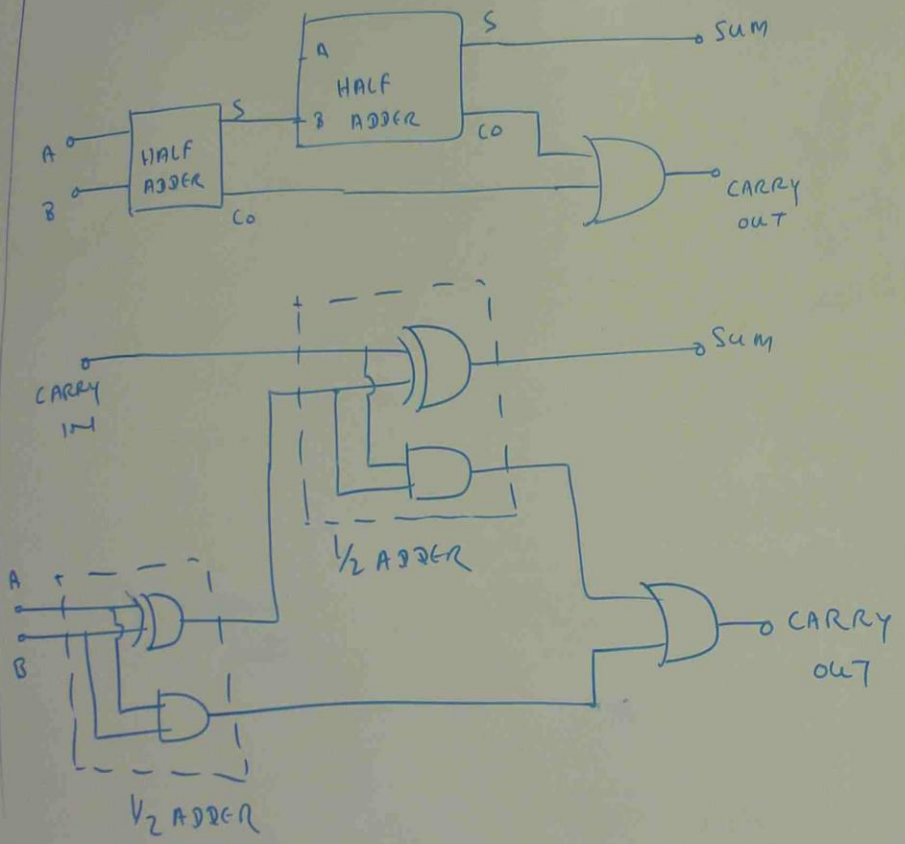


HALF ADDER CAN ONLY ADD TWO BINARY BITS. IT DOES NOT ALLOW FOR A CARRY IN FROM

FULL ADDER



FULL ADDER



TRUTH TABLE OF FULL ADDER

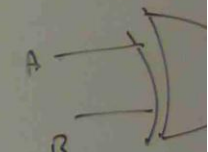
INPUTS			OUTPUTS	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

FULL ADDER

USE FOR 4 BIT BINARY NUMBER.

EX-OR

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0



ICs

GATE TYP

AND
OR
NAND
NOR
EX OR

S)

(CO)

ADD TWO

ALLOW FOR A CARRY IN FROM PREVIOUS ADDITION

SUM

CARRY OUT

SUM

CARRY OUT

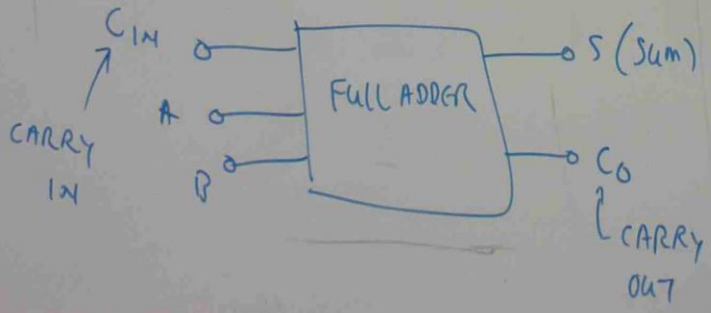
TION

TRUTH TABLE OF FULL ADDER

INPUTS			OUTPUTS	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

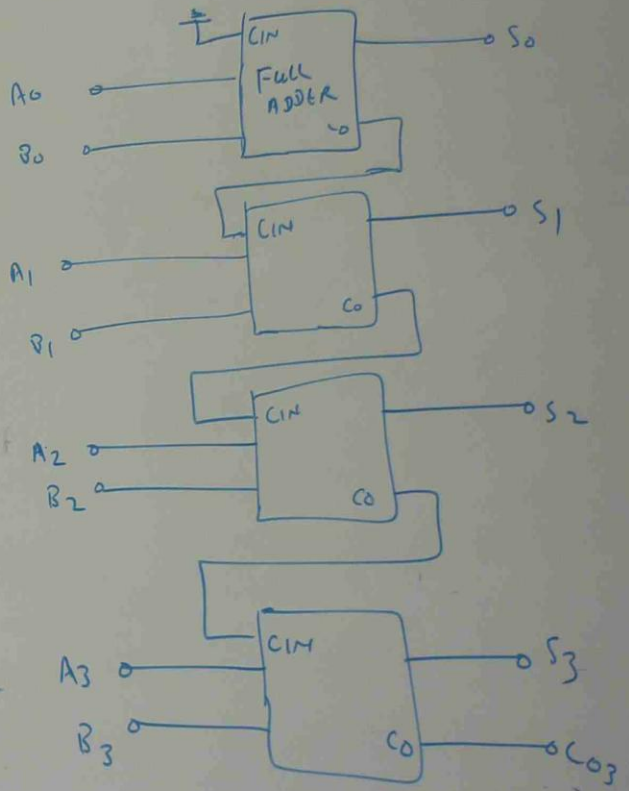
FULL ADDER

USE FOR 4 BIT BINARY NUMBER.



CASCADING

CASCADING 4 FULL ADDERS TO ADD TWO, 4 BIT BINARY NUMBERS.



ENCODERS & DECODERS

ANY DATA WITH IN A DIGITAL CIRCUIT IS COMPRISED of "1S" AND "0S", ALTHOUGH AN OUTPUT DEVICE MAY DISPLAY THE DATA IN VARIOUS FORMS, SUCH AS THE OCTAL (OR) HEXADECIMAL FORM.

IN PUT DEVICES TO A DIGITAL CIRCUIT, SUCH AS KEY BOARD (OR) A DIGITAL TRANSDUCER WILL INPUT THE BINARY INFORMATION IN A FORM OTHER THAN STRAIGHT BINARY : THAT IS, AS A CODE.

TO CHANGE THE BINARY DATA CODES FROM ONE FORM TO ANOTHER, DECODERS AND ENCODERS ARE USED.

DECIM
0
1
2
3
4
5
6
7
8
9

BCD BINARY CODED DECIMAL

$23_{10} = 0010\ 0011$ (BCD)

$2579_{10} = 0010\ 0101\ 0111\ 1001$ (BCD)

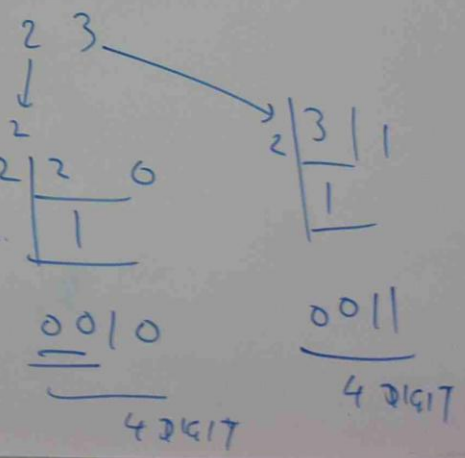
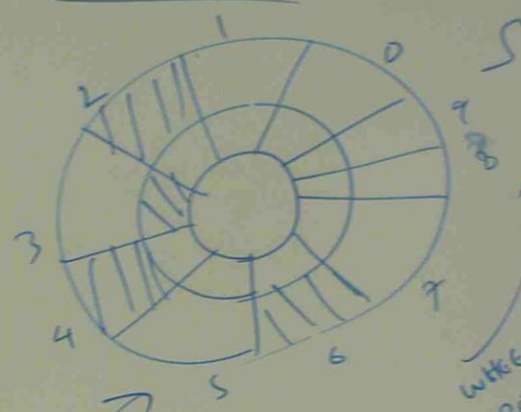


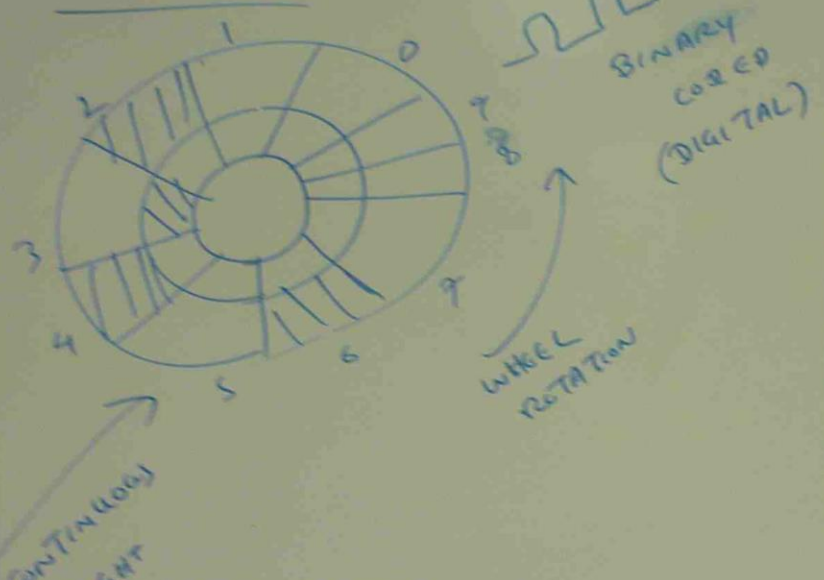
TABLE DECIMAL → BCD

DECIMAL	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

GRAY CODE



GRAY CODE



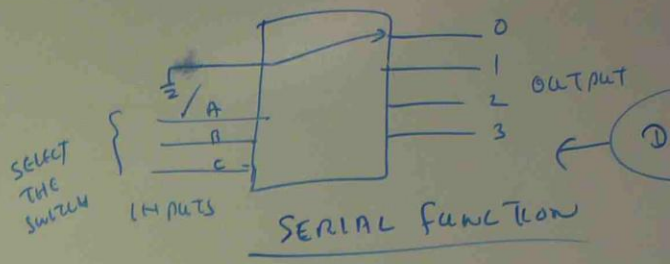
ANALOG

GRAY CODE TABLE

DECIMAL	BINARY	GRAY CODE
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

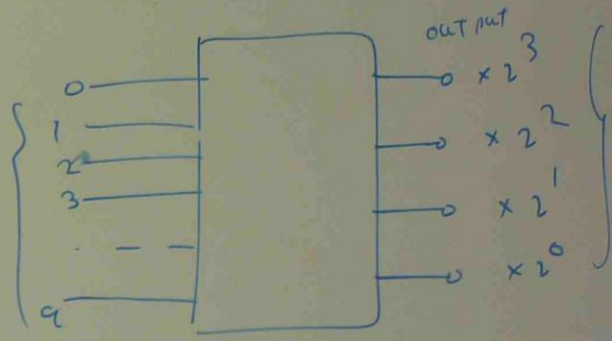
DECODER AND ENCODER

A DECODER IS DEFINED AS A DEVICE THAT HAS A NUMBER of INPUTS AND OUTPUTS, BUT ACTIVATES ONLY ONE OUTPUT FOR A GIVEN INPUT CODE



SERIAL FUNCTION

AN ENCODER IS A DEVICE THAT HAS A NUMBER OF INPUTS AND OUTPUTS BUT PRODUCES A SPECIFIC CODE AT THE OUTPUT WHEN ONLY ONE INPUT AT A TIME IS ACTIVATED.



$1011 \longrightarrow 1\times 2^3 + 0\times 2^2$

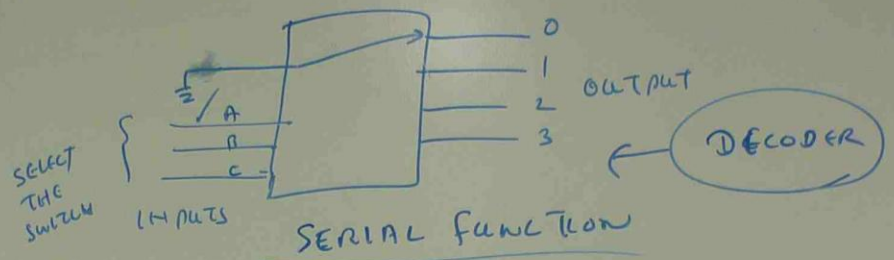
INPUT $= 8 + 0$

$= 11$

PARALLEL FUNCTION

AS A DEVICE THAT HAS A NUMBER OF

BUT ACTIVATES ONLY ONE OUTPUT FOR

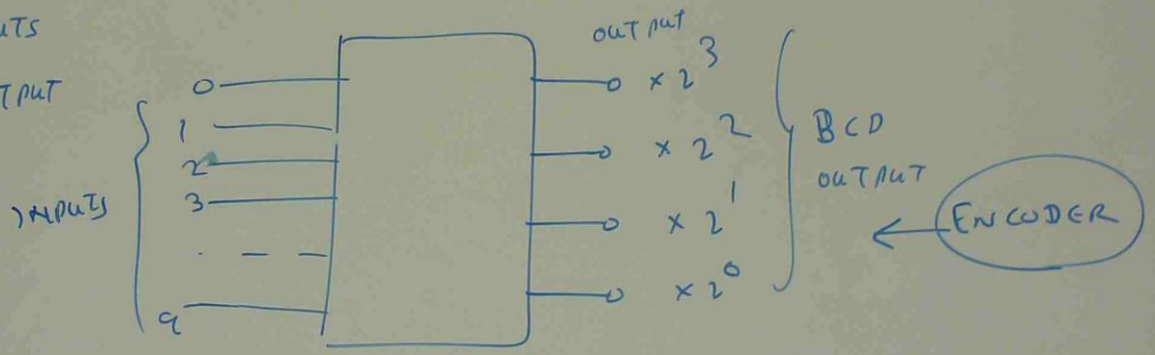


SERIAL FUNCTION

CE THAT HAS A NUMBER OF INPUTS

RODUCES A SPECIFIC CODE AT THE OUTPUT

AT A TIME IS ACTIVATED.



$1011 \longrightarrow 1\times2^3+0\times2^2+1\times2^1+1\times2^0$

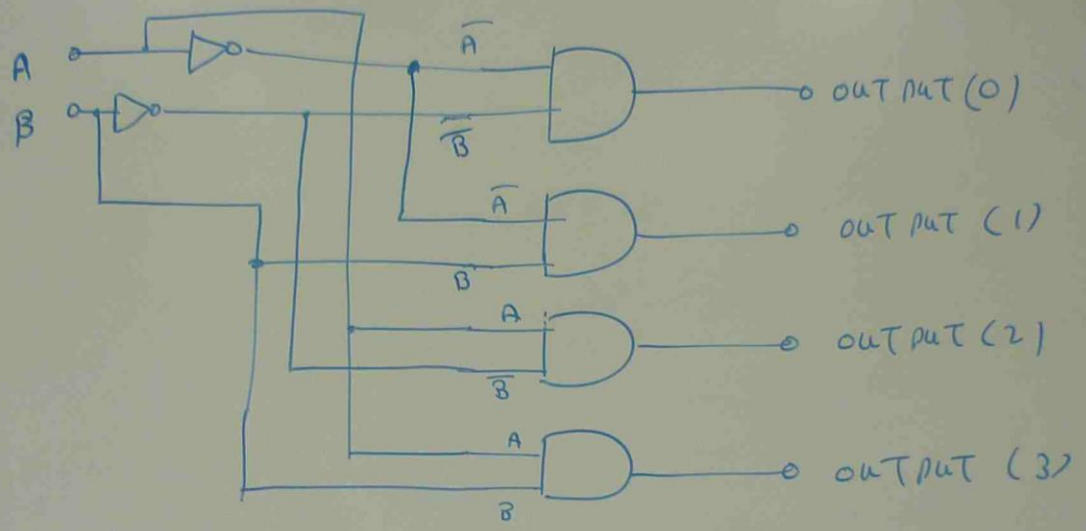
INPUT

$= 8+0+2+1$

PARALLEL $= 11$

FUNCTION

CONSTRUCTING A DECODER BY DIGITAL GATES



THERMO COUPLES

TYPE	MATERIAL (+)	MATERIAL (−)	ΔV/°C AT 100°C (μV)	USABLE RANGE (°C)	COMMENT
E	CHROMEL (90% NICKEL, 10% CHROMIUM)	CONSTANTAN (57% COPPER, 43% NICKEL)	68	0 TO 800	HIGHEST OUTPUT THERMO COUPLE
T	COPPER	CONSTANTAN	46	−185 TO +300	USED FOR MILDLY OXIDISING ATMOSPHERE
K	CHROMEL	ALUMEL 94% NICKEL, 3% MANGANESE 2% ALUMINIUM 1% SILICON	42	0 TO 1100	GENERAL PURPOSE WIDELY USED
J	IRON	CONSTANTAN	46	20 TO 700	USED WITH REDUCING ATMOSPHERE
R/S	PLATINUM/13% RHODIUM PLATINUM		8	0 TO 1600	HIGH TEMPERATURE
V/U	COPPER	COPPER/NICKEL	—	—	COMPENSATING CABLE UP TO 50°C

	COMMENT
	HIGHEST OUT PUT THERMO COUPLE
	USED FOR MILDLY OXIDISING ATMOSPHERE
	GENERAL PURPOSE WIDELY USED
	USED WITH REDUCING ATMOSPHERE
O	HIGH TEMPERATURE
	COMPENSATING CABLE UP TO 50°C

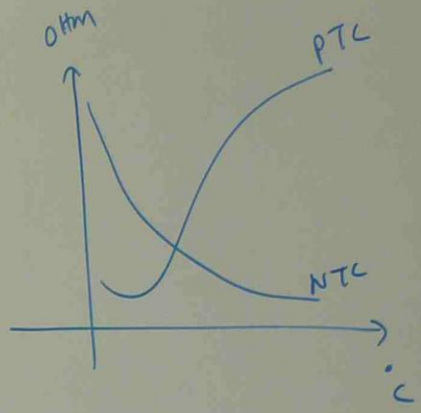
THERMISTOR

THESE ARE TEMPERATURE DEPENDENT RESISTORS. THEIR RESISTANCE IS DETERMINED BY THEIR TEMPERATURE.

TWO BASIC TYPES

PURE METAL

METAL OXIDE



PURE METAL

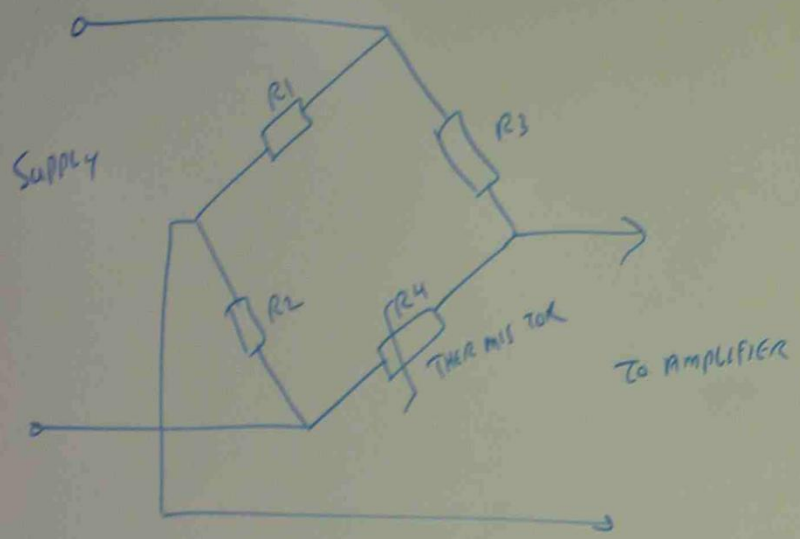
RESISTANCE TEMPERATURE DETECTOR (RTD).

METAL OXIDE

→ POSITIVE TEMPERATURE COEFFICIENT (PTC)
RESISTANCE DECREASES FOR A TEMPERATURE DECREASES

→ NEGATIVE TEMPERATURE COEFFICIENT (NTC)
RESISTANCE DECREASES FOR A TEMPERATURE INCREASES

RESISTANCE RANGE FOR THERMISTOR	10Ω → 1MΩ (STANDARD)	100Ω → 100KΩ (MEASUREMENT)	REFERENCE RESISTANCE OHMS AT 25°C



ADVANTAGES

SMALL SIZE

FAST RESPONSE

DISADVANTAGES

POOR LINEARITY

LIMITED RANGE

APPLICATIONS

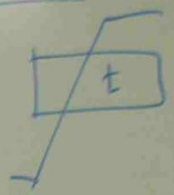
MOTOR PROTECTION

TEMPERATURE MONITORING

MEAT COOKING SENSING

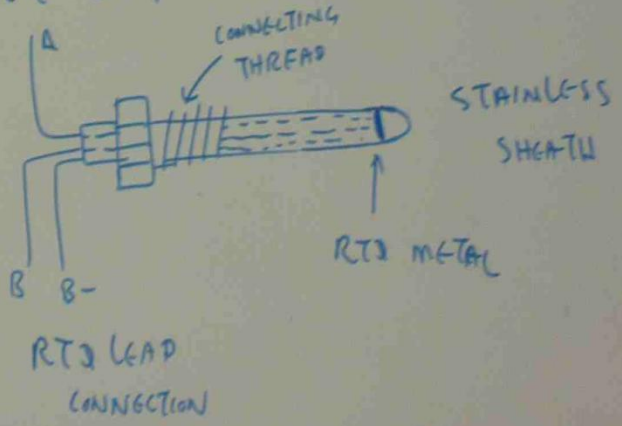
ENGING EXHAUST TEMPERATURE SENSING

RTD



THE RESISTANCE TEMPERATURE DETECTOR IS A PURE METAL THERMISTOR. THEY HAVE A POSITIVE TEMPERATURE COEFFICIENT (PTC).

INDUSTRIAL STYLE THERMISTORS ARE OFTEN CONSTRUCTED IN A STAINLESS STEEL SHEET TO PROTECT THE EXPENSIVE DETECTORS.



ENCODERS AND DECODER

SERIAL DATA

A DATA TRANSFER METHOD IN WHICH EACH BIT IS FED SEQUENTIALLY OVER A SINGLE TRANSMISSION LINE

PARALLEL DATA

A DATA TRANSFER METHOD WHERE DATA IS TRANSFERRED OVER A NUMBER OF LINES.

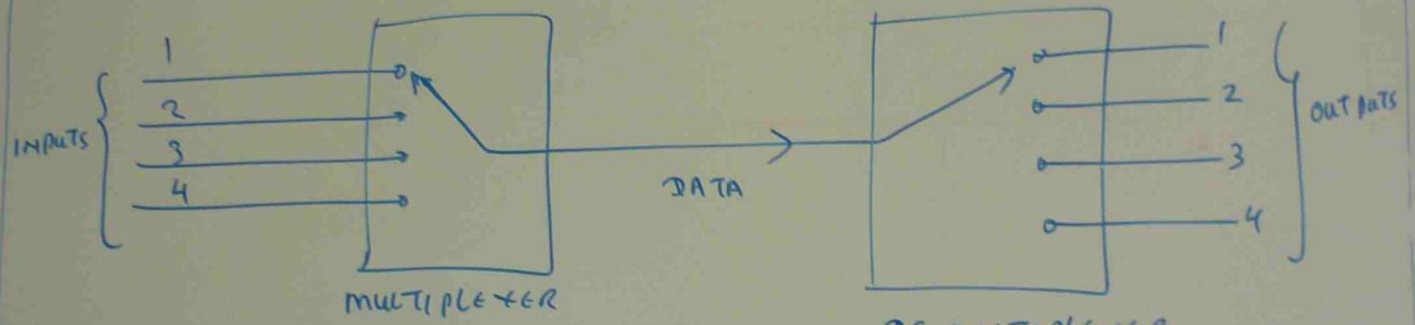
ASCII CODE (AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE)

- 7 BIT CODE FOR ALL ALPHA NUMERIC CHARACTERS ON TYPE WRITER.
- USED FOR SENDING TEXT BETWEEN COMPUTERS, PRINTERS, WORD PROCESSORS ETC.

CHARACTER	ASCII CODE	
	BINARY	HEX
A	100 0001	41
B	100 0010	42
a	110 0001	61
0	011 0000	30
9	011 1001	39
SPACE	010 0000	20

MULTIPLEXERS

A SPECIAL USE OF DECODER / ENCODER ICS IS MULTIPLEXING WHICH, IN AN ELECTRICAL SENSE, MEANS USING ONE DATA LINE TO TRANSMIT SEVERAL SIGNALS; APPARENTLY SIMULTANEOUSLY.



MULTIPLEXER
(DATA SELECTOR)

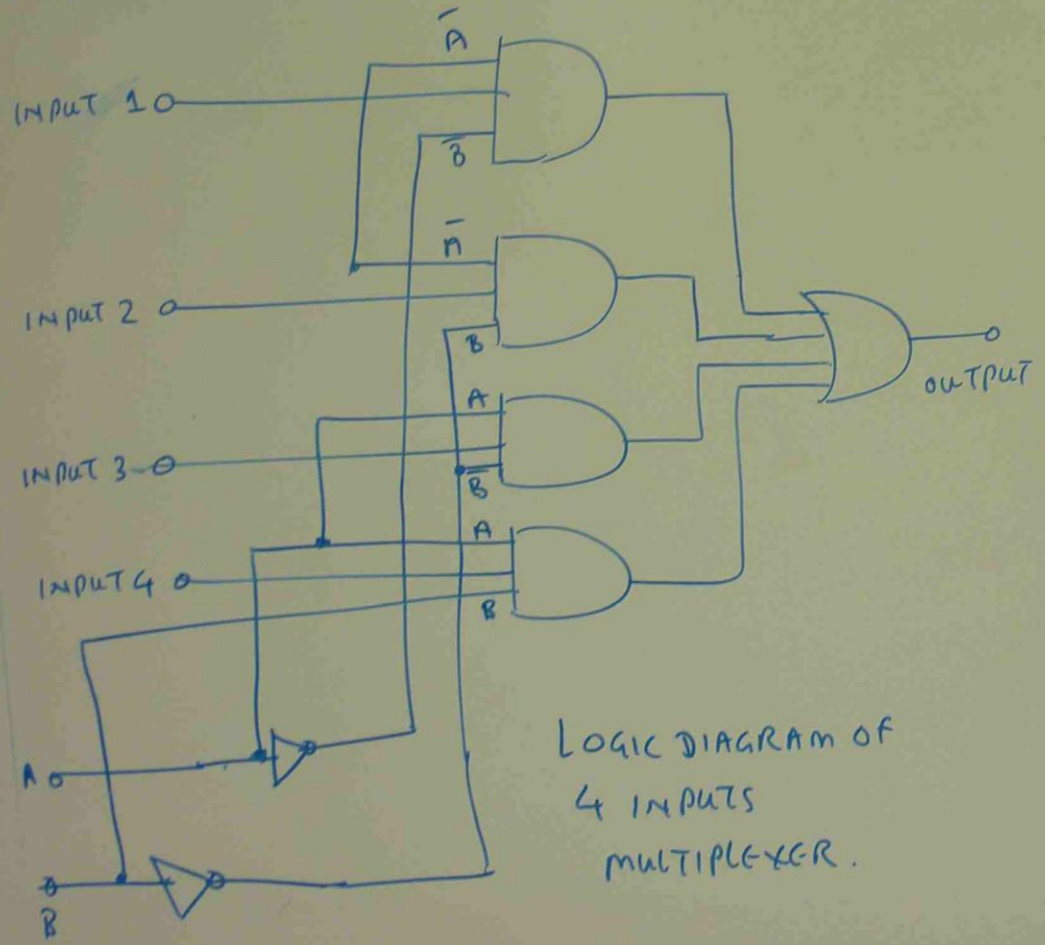
DE MULTIPLEXER
(DATA DISTRIBUTOR)

(4 POLES SINGLE WAY SWITCH)

MULTIPLEXING IS OFTEN USED IN COMPUTERS TO TRANSMIT DATA OVER A SINGLE LINE. (Eg. PRINTED CIRCUIT BOARD TRACK)

MULTIPLEXER (DATA SELECTOR)

– A FORM OF ENCODER

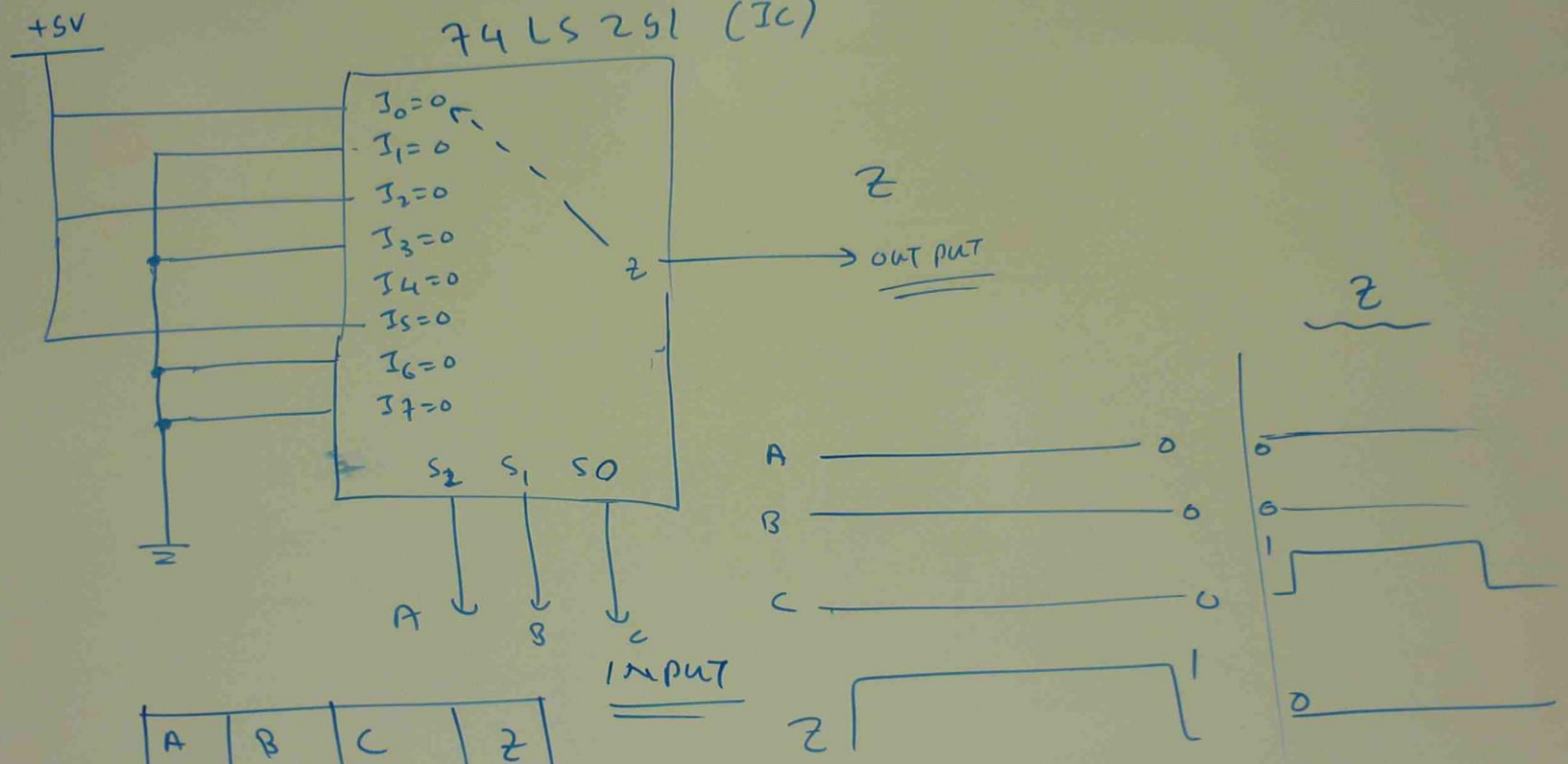


LOGIC DIAGRAM OF 4 INPUTS MULTIPLEXER.

MULTIPLEXER IC

TYPE	DEVICE	OUTPUT	
QUAD 2 INPUT	74LS157	TRUE	
QUAD 2 INPUT	74LS158	OUTPUT INVERTED	
QUAD 2 INPUT	74LS257	TRUE	
QUAD 2 INPUT	74LS258	INVERTED	
QUAD 2 INPUT	74LS298	LATCHED	
DUAL 4 INPUT	74LS153	TRUE	
DUAL 4 INPUT	74LS253	TRUE	
DUAL 4 INPUT	74LS352	INVERT	
DUAL 4 INPUT	74LS353	INVERT	
8 INPUT	74LS151	INVERT + TRUE	
8 INPUT	74LS251	INVERT	+ TRUE
8 INPUT	74LS152	INVERT	
16 INPUT	74150	INVERT	

TRANSFERRING DIGITAL DATA ALONG A COMMON DATA LINE → USE MULTIPLEXER



A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	1	0	0
1	1	1	0

FLIP FLOP

COMBINATIONAL LOGIC – MULTIPLEXER / DE-MULTIPLEXER (NO MEMORY)

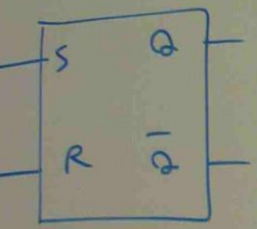
OUTPUT REMAINS STEADY AS LONG AS INPUT CONDITIONS REMAIN CONSTANT

SEQUENTIAL LOGIC – UTILIZE MEMORY DEVICE

SEQUENTIAL DIGITAL SYSTEM.

FUNDAMENTAL ELEMENT of SEQUENTIAL LOGIC IS FLIP FLOP

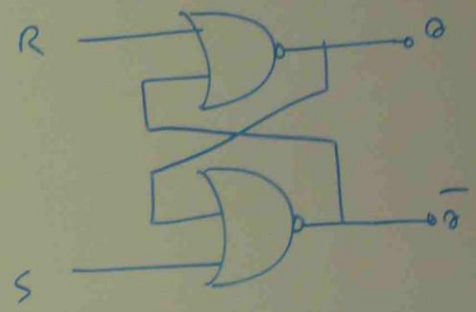
INPUT | OUTPUT | SET/RESET DEVICE (SR)



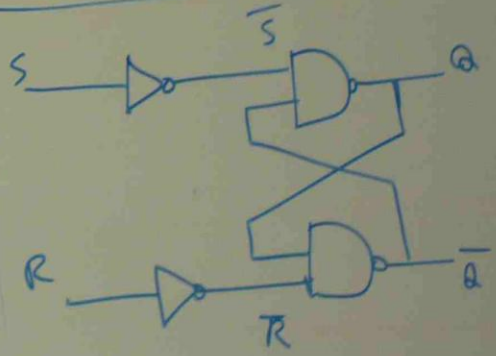
TRUTH TABLE

INPUTS		OUTPUT		RESULT
S	R	Q	$\bar{Q}$	
INACTIVE	INACTIVE	X	X	NO CHANGE
ACTIVE	INACTIVE	1	0	SET
INACTIVE	ACTIVE	0	1	RESET
ACTIVE	ACTIVE	UNDEFINED		INVALID

NOR GATE S R FLIP FLOP



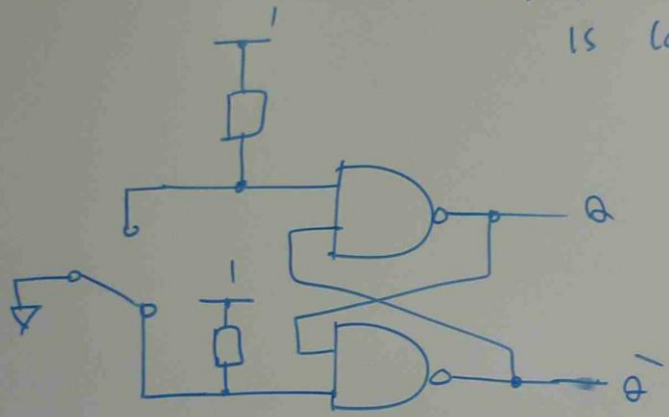
NAND GATE SR FLIP FLOP



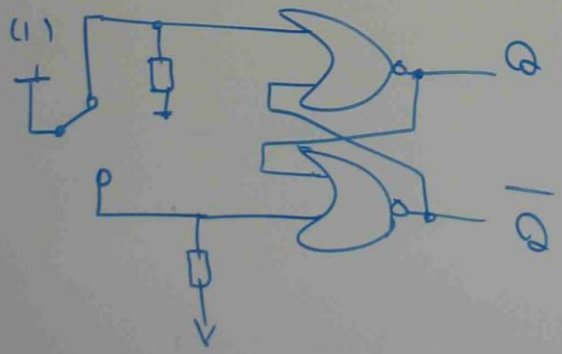
NAND RS FLIP FLOP TO DE BOUNCE SWITCH

SINGLE POLE DOUBLE THROW TYPE (SPDT)

PULL UP RESISTORS ⟶ OPEN CIRCUIT INPUT IS LOGIC 1



DE BOUNCING SWITCH WITH NAND GATE

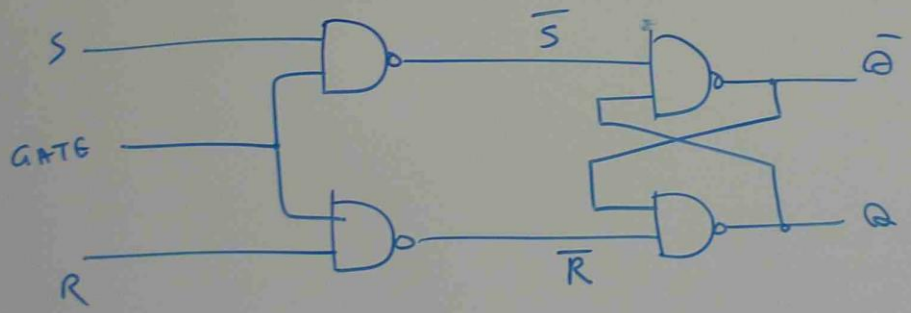


DE BOUNCING SWITCH WITH NOR GATE

GATED SR LATCH ⟶ CLOCKED R S FLIP FLOP

THE BASIC SR FLIP FLOP RESPONDS TO ITS INPUTS DIRECTLY WHICH IN MANY INSTANCES CAUSE TIMING PROBLEMS.

TO OVERCOME THIS IS A CLOCKED SR FLIP FLOP USED TO STORE THE DATA. (STATE OF THE SET (OR) RESET TERMINALS) ONLY WHEN THE FLIP FLOP IS ENABLED BY ANOTHER SIGNAL CALLED CLOCK SIGNAL.



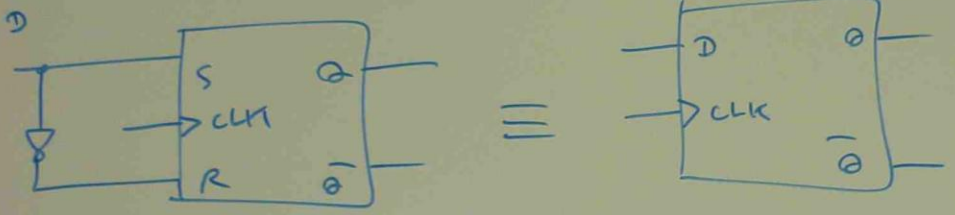
THE SR DATA IS PASSED ONTO FLIP FLOP ONLY WHEN THE GATE (OR) ENABLE SIGNAL IS A LOGIC 1. THE FLIPFLOP WILL STORE THE R S DATA EXISTING AT THE INSTANT THE ENABLE SIGNAL IS REMOVED.

DEVELOPMENT OF FLIP FLOP

SR FLIP FLOP IS NOT A COMMONLY USED DEVICE BECAUSE IT HAS INVALID STATE.

D, T, K FLIP FLOPS ARE DEVELOPED TO OVERCOME THE PROBLEM

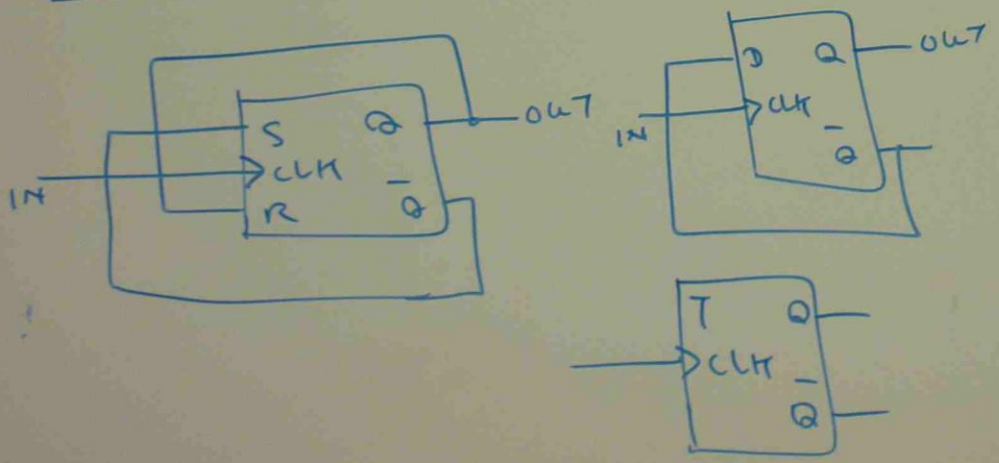
D FLIP FLOP



D FLIP FLOP TRUTH TABLE

	D	Q_n	Q_{n+1}	
1	0	0	0	RESET
2	0	1	0	
3	1	0	1	SET
4	1	1	1	

TOGGLE (T) FLIP FLOP



J-K FLIP FLOP

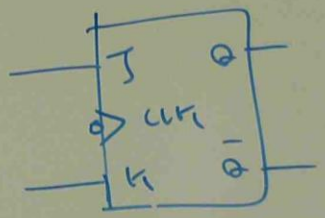
THE J-K FLIP FLOP OVERCOMES THE PROBLEM OF THE POSSIBLE INVALID OUTPUT CONDITION IN S-R FLIP FLOP WHILE STILL RETAINING TWO INPUTS.

THE SET INPUT IS NOW J INPUT. THE RESET INPUT IS NOW THE K INPUT.

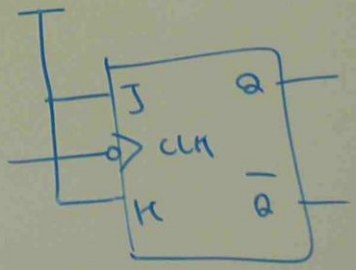
IF BOTH THE J AND K INPUTS ARE HELD AT A LOGIC 1, THE OUTPUTS WILL TOGGLE RATHER THAN BECOME INDETERMINE

JK FLIP FLOP TRUTH TABLE

	J	K	Q	Q$_{n+1}$	
1	0	0	0	0	NO CHANGE
2	0	0	1	1	
3	0	1	0	0	RESET
4	0	1	1	0	
5	1	0	0	1	SET
6	1	0	1	1	
7	1	1	0	1	TOGGLE
8	1	1	1	0	

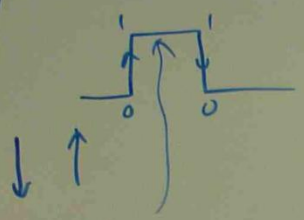


JK FLIP FLOP
(NEGATIVE EDGE TRIGGERED)



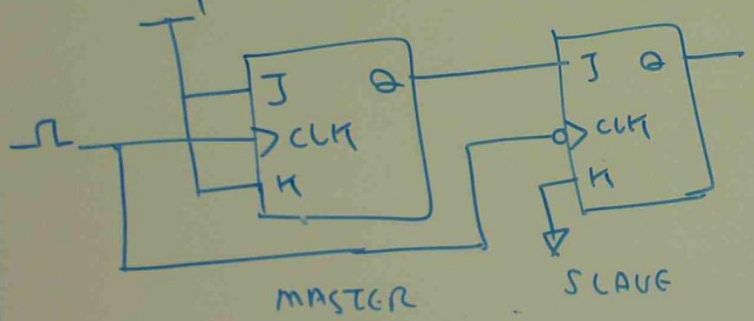
T FLIP FLOP FROM JK FLIP FLOP

MASTER - SLAVE FLIP FLOP



CONNECTING CONVENTIONAL J-K FLIP FLOP CAN GIVE THE PROBLEMS DUE TO TIME DELAY

THE PROBLEMS CAN ARISE FROM THE FACT THAT ALTHOUGH THE FLIP FLOP CHANGES ON THE EDGE OF IT'S CLOCK SIGNAL, THERE IS A SMALL TIME INTERVAL BEFORE AND AFTER THE CLOCK EDGE DURING WHICH THE INPUT DATA MUST BE HELD STABLE. THESE TIMES ARE CALLED SET UP & HOLD TIMES RESPECTIVELY.



WHEN THE CLOCK IS HIGH

MASTER IS ENABLED) SLAVE IS DISABLED

MASTER OUTPUT WILL BE SET ACCORDING TO DATA PRESENTS AT MASTER'S INPUT) SLAVE FLIP FLOP REMAINS UNCHANGED

WHEN THE CLOCK SIGNAL RETURNS TO ZERO

SLAVE FLIP FLOP WILL RESPOND TO THE OUTPUT OF MASTER.

TRUTH DIAGRAMS OF EDGE TRIGGERED FLIP FLOP AND MASTER SLAVE FLIP FLOP

INPUT			OUTPUT	
CLK	J	K	Q	$\bar{Q}$
↓	L	L	Q_0	$\bar{Q}_0$
↓	H	L	H	L
↓	L	H	L	H
↓	H	H	TOGGLE	

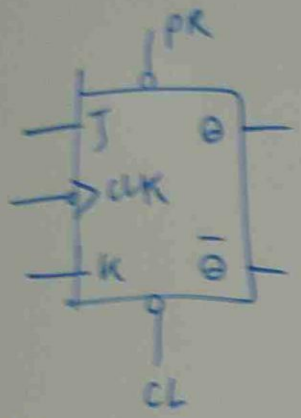
EDGE TRIGGERED FLIP-FLOP

INPUT			OUTPUT	
CLK	J	K	Q	$\bar{Q}$
⊓	L	L	Q_0	$\bar{Q}_0$
⊓	H	L	H	L
⊓	L	H	L	H
⊓	H	H	TOGGLE	

MASTER-SLAVE FLIP FLOP

ANGED

JK FLIP FLOP WITH ASYNCHRONOUS PRESET AND CLEAR



PR - PRESET

CL - CLEAR

INPUTS					OUTPUTS	
PR	CL	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

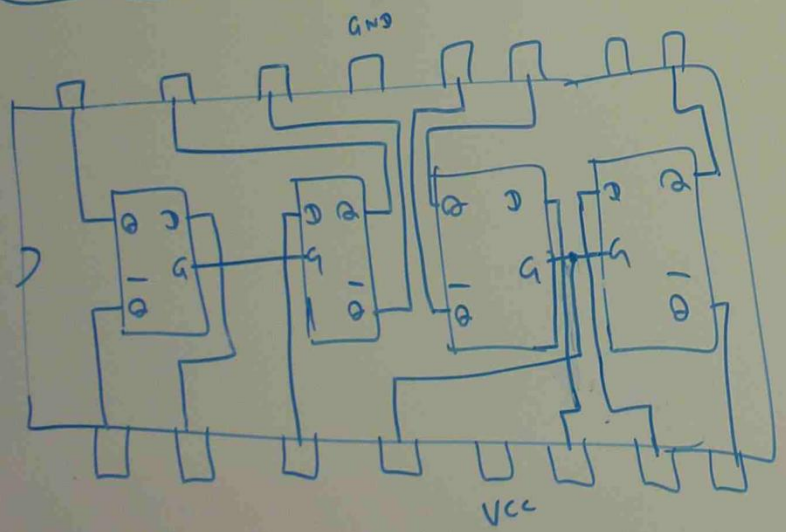
SHIFT REGISTERS AND DATA LATCHES

FLIP FLOPS ARE USED IN A VARIETY OF APPLICATIONS INCLUDING THE LATCH AND SHIFT REGISTER FUNCTIONS.

- FLIP FLOP → STORE 1 BIT OF DATA

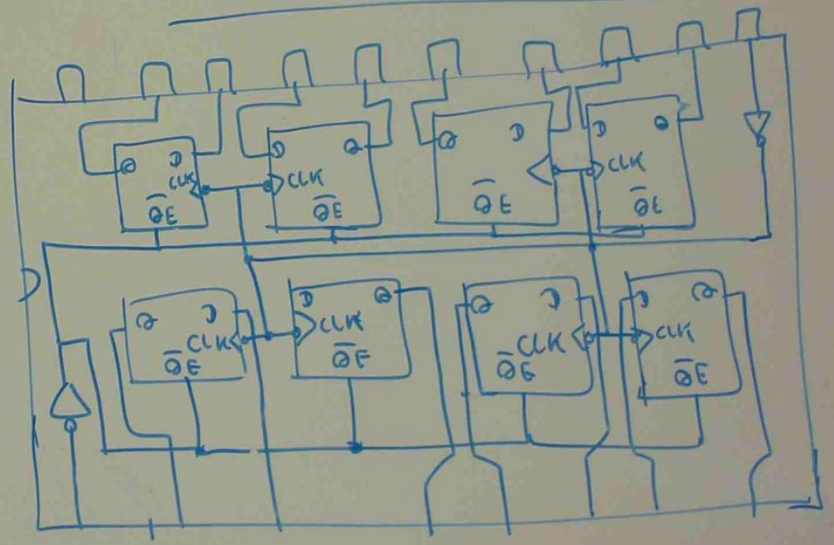
LATCH → INTER CONNECTION OF FLIP FLOPS → CAN STORE SEVERAL BITS OF DATA

4 BIT LATCH → 4 FLIP FLOP – STORE 4 BIT DATA



74 LS 75 4 BIT LATCH

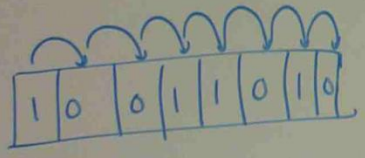
8 BIT LATCH – STORE 8 BIT DATA



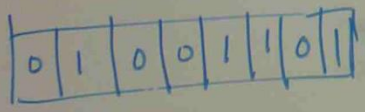
74 LS 374 OCTAL D TYPE LATCH

SHIFT REGISTERS

MANY DIGITAL APPLICATIONS REQUIRE THAT BINARY DATA BE SHIFTED EITHER TO LEFT (OR) RIGHT

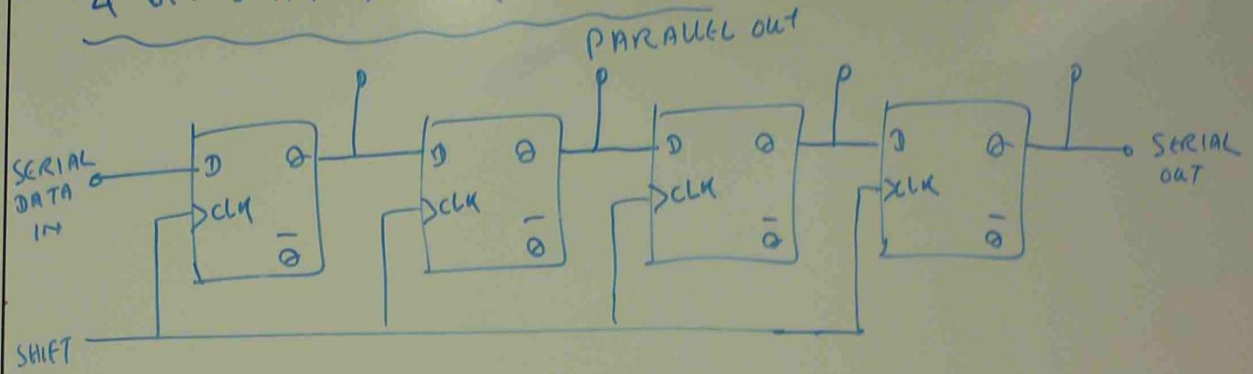


154_{10}

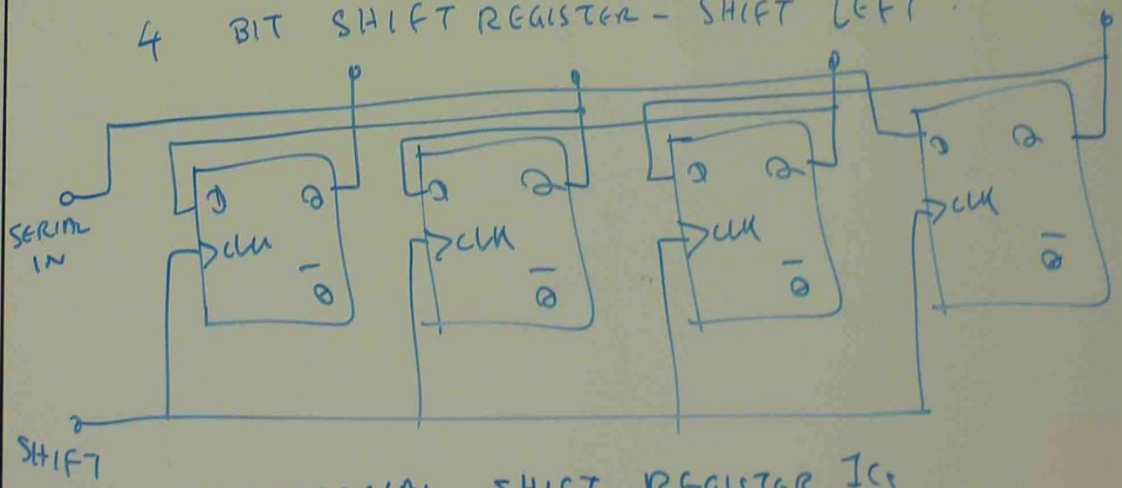


77_{10}

4 BIT SHIFT REGISTER – SHIFT RIGHT



4 BIT SHIFT REGISTER – SHIFT LEFT



COMMERCIAL SHIFT REGISTER ICs

TTL 74LS194, CMOS 4194 } (16 PIN 4 REGISTERS)

COUNTERS

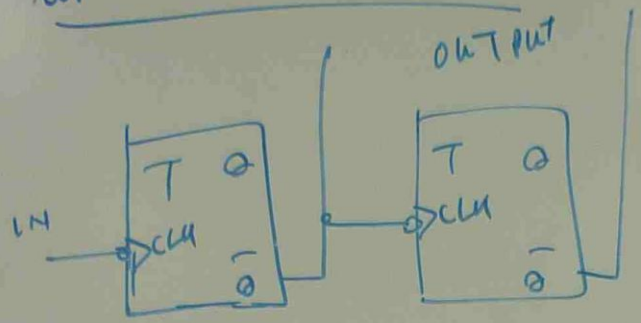
- COUNTERS CAN BE USED TO COUNT THE NUMBER OF ITEMS ON A CONVEYOR (OR) IF USED TO COUNT THE NUMBER OF PULSES FROM A SHAFT ENCODER CAN INDICATE THE ROTARY POSITION OF A SHAFT (OR) X-Y POSITION OF MACHINING BEDS
- FLIP FLOPS ARE CONNECTED AS COUNTERS
- COUNTER PRODUCES A SERIES OF BINARY NUMBERS STARTING AT A PRESET VALUE (OFTEN 0) CYCLING AT A RATE DETERMINED BY THE INPUT CLOCK.

DECIMAL	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

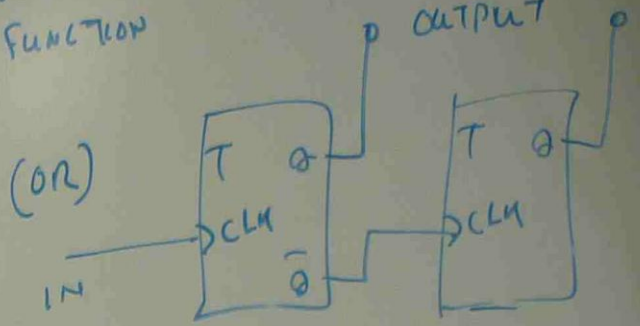
(LSB - LEAST SIGNIFICANT BIT)

3 BITS BANARY COUNTER

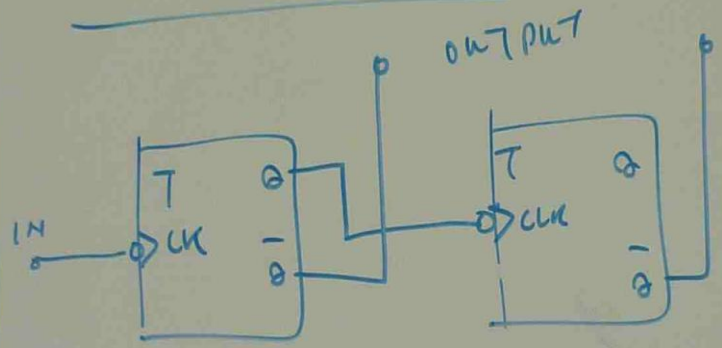
UP COUNTER 0 1 2 3



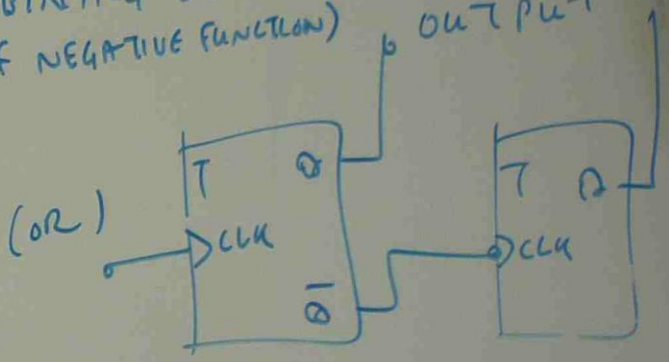
COMBINING ODD NUMBER OF NEGATIVE FUNCTION



DOWN COUNTER 3 2 1 0



(COMBINING EVEN NUMBER OF NEGATIVE FUNCTION)

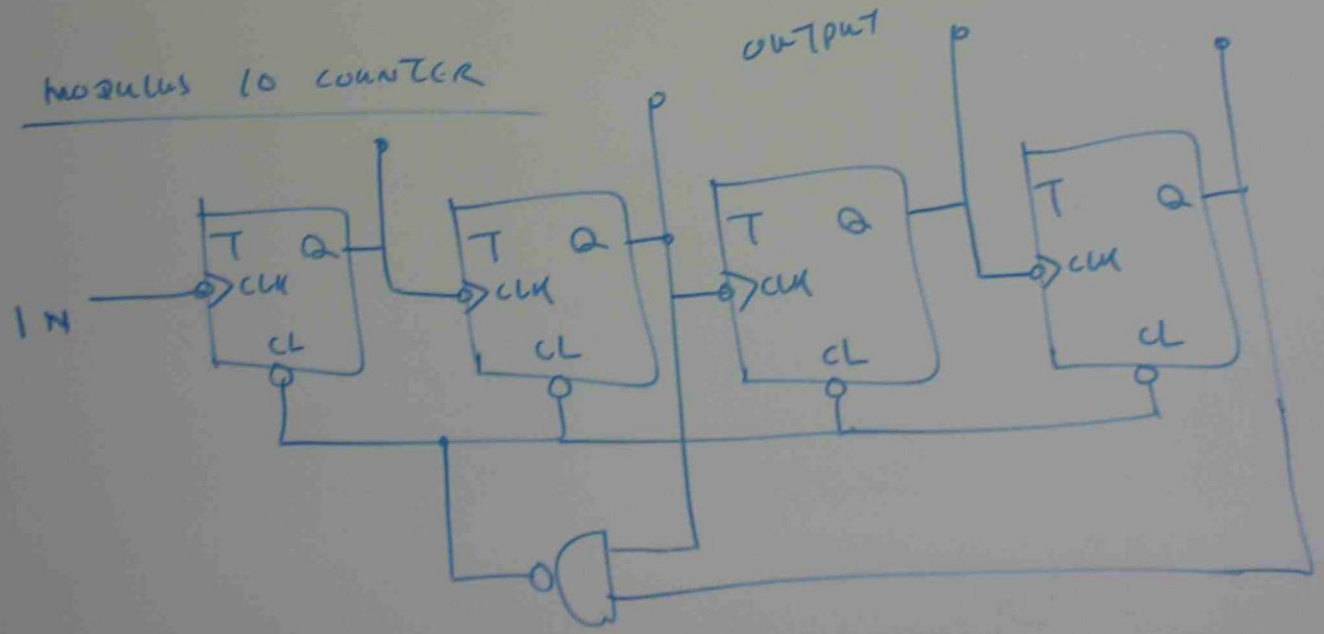


MODULUS of A COUNTER

THE MODULUS of A COUNTER REFERS TO THE NUMBER of THE STATES THAT THE COUNTER CAN OUTPUT

0 ⟶ 15 COUNTER HAS 16 STATES. IT IS MODULO 16 COUNTER

MODULUS 10 COUNTER

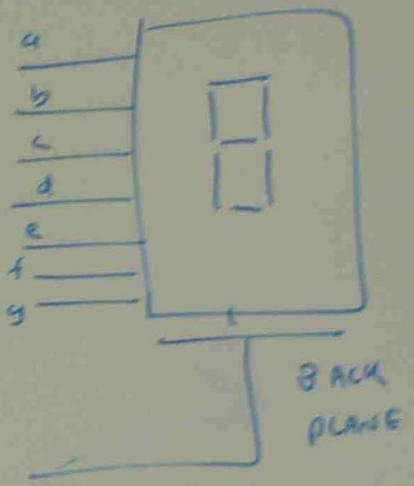


COUNTER ICS

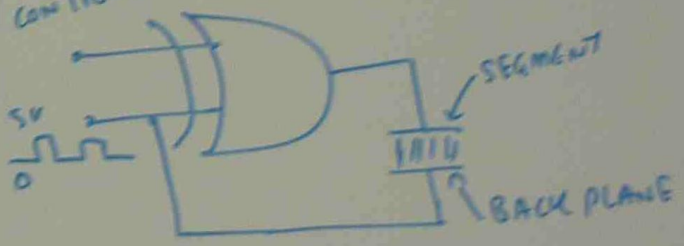
TYPE	MODULUS	CLOCK FREQUENCY
74LS90	2 x 5	32 MHz
74LS92	2 x 6	32 MHz
74LS93	2 x 8	32 MHz
74LS390	2 x 5	40 MHz
4020	16384	10 MHz
4024	128	12 MHz

7 SEGMENT DISPLAY

LCD DISPLAY

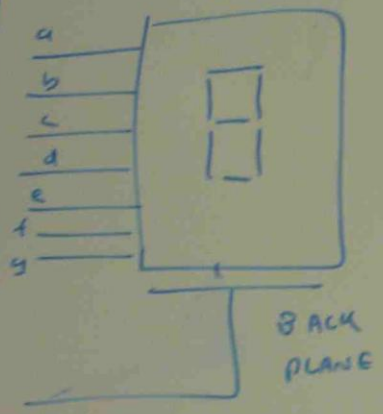


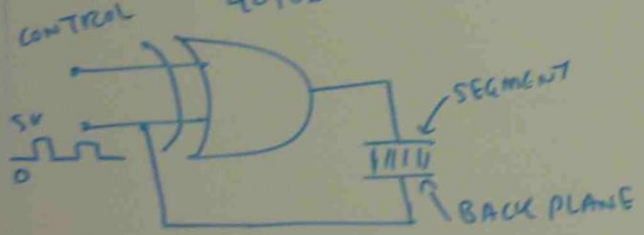
4070B



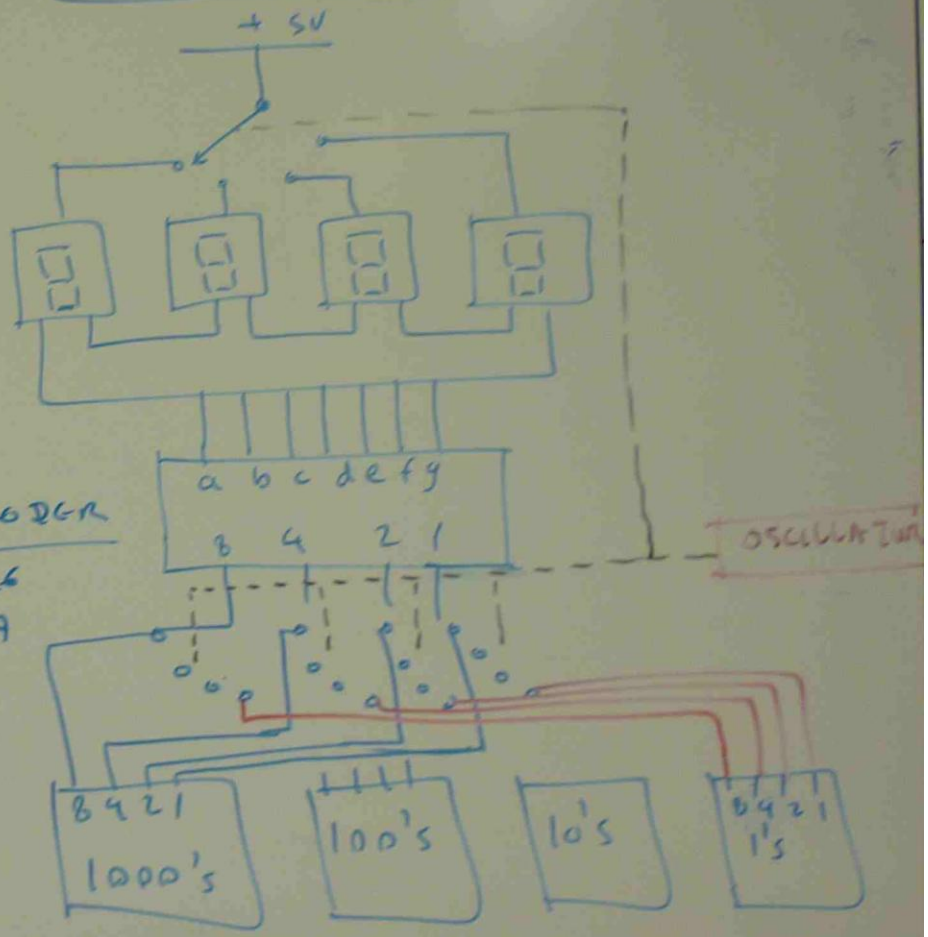
7 SEGMENT DISPLAY

LCD DISPLAY



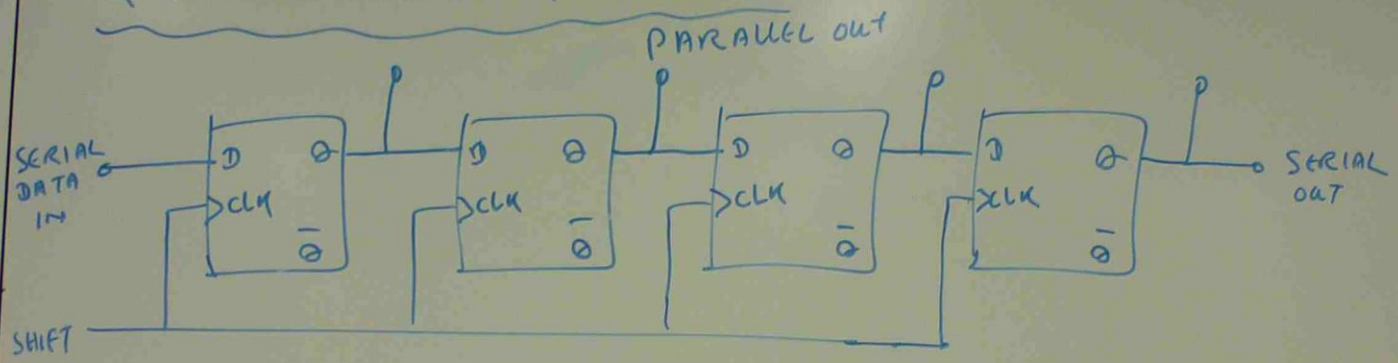


MULTIPLEXED LCD DISPLAY

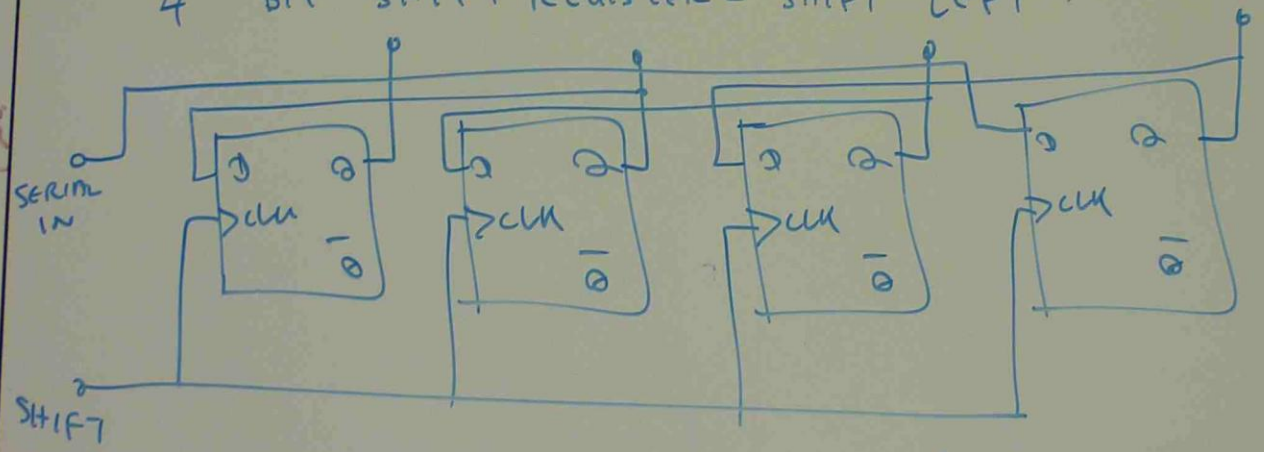


MULTIPLEXING 7 SEGMENT LCD DISPLAY.

4 BIT SHIFT REGISTER – SHIFT RIGHT



4 BIT SHIFT REGISTER – SHIFT LEFT



COMMERCIAL SHIFT REGISTER ICs

TTL 74LS194, CMOS 4194 } (16 PIN 4 REGISTERS)

COUNTERS

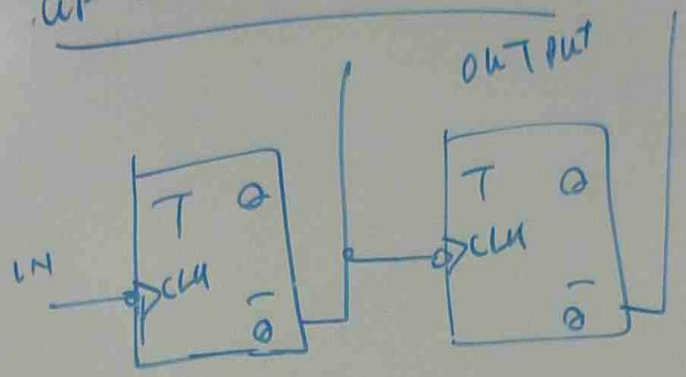
- COUNTERS CAN BE USED TO COUNT THE NUMBER OF ITEMS ON A CONVEYOR (OR) IF USED TO COUNT THE NUMBER OF PULSES FROM A SHAFT ENCODER CAN INDICATE THE ROTARY POSITION OF A SHAFT (OR) X–Y POSITION OF MACHINING BEDS
- FLIP FLOPS ARE CONNECTED AS COUNTERS
- COUNTER PRODUCES A SERIES OF BINARY NUMBERS STARTING AT A PRESET VALUE (OFTEN 0) CYCLING AT A RATE DETERMINED BY THE INPUT CLOCK.

DECIMAL	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

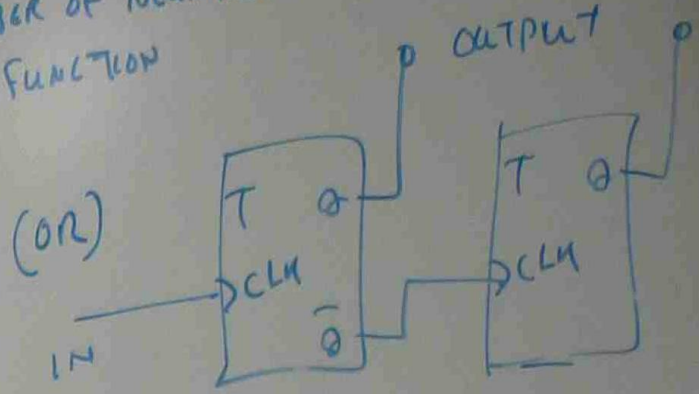
(LSB - LEAST SIGNIFICANT BIT)

3 BITS BANARY COUNTER

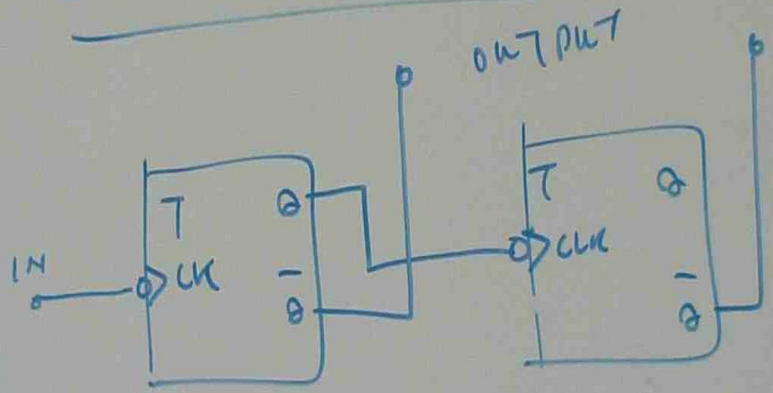
UP COUNTER 0 1 2 3



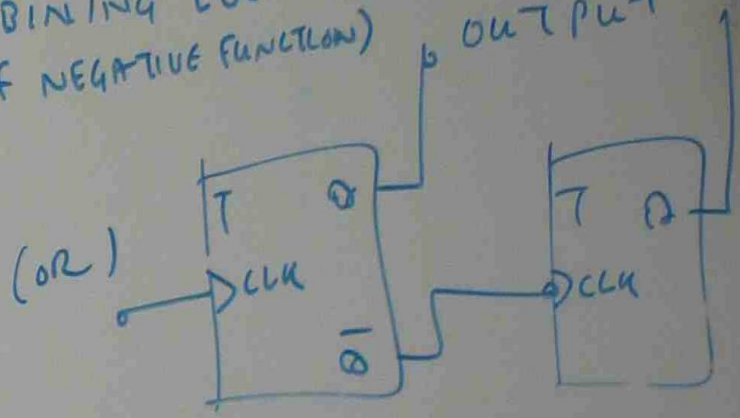
COMBINING ODD NUMBER OF NEGATIVE FUNCTION



DOWN COUNTER 3 2 1 0



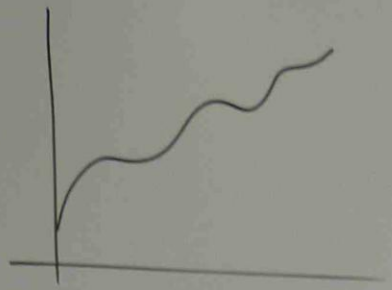
(COMBINING EVEN NUMBER OF NEGATIVE FUNCTION)



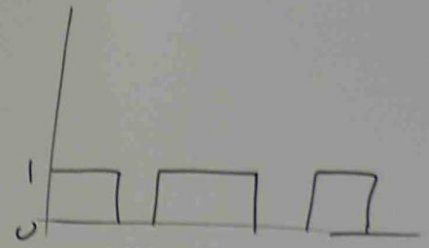
1096

DIGITAL SIGNAL PROCESSING AND CONDITIONING

ANALOG SIGNAL



DIGITAL SIGNAL



ANALOG INFORMATION (OR) ANALOG SIGNALS ARE SUBJECT TO ELECTRICAL NOISE, INTERFERENCE, DRIFT, AMPLIFIER GAIN, LOADING EFFECT ETC.

IN A DIGITALLY ENCODED SIGNAL, A WIRE CARRIES EITHER A HIGH (OR) LOW LEVEL AND IS NOT PARTICULARLY SUSPECTIBLE TO THE PROBLEMS ASSOCIATED WITH ANALOG SIGNAL PROCESSING.

DIGITAL COMPUTER REQUIRES INFORMATION ENCODED IN DIGITAL FORMAT BEFORE IT CAN BE USED.

NUMBER SYSTEM

BINARY —— BASE "2"
OCTAL —— BASE "8"
HEX DECIMAL —— BASE "16"

BINARY

$$N_{10} = a_n \times 2^n + a_{n-1} 2^{n-1} + \cdots a_3 2^3 + a_2 2^2 + a_1 2^1 + a_0 2^0$$

N_{10} = BASE 10 NUMBER — DECIMAL

N_2 = BASE 2 NUMBER — BINARY

Pb FIND THE BINARY EQUIVALENT OF 259_{10}

$259/2 = 129 + 1/2 \longrightarrow a_0 = 1$
$129/2 = 64 + 1/2 \longrightarrow a_1 = 1$
$64/2 = 32 + 0 \longrightarrow a_2 = 0$
$32/2 = 16 + 0 \longrightarrow a_3 = 0$
$16/2 = 8 + 0 \longrightarrow a_4 = 0$
$8/2 = 4 + 0 \longrightarrow a_5 = 0$
$4/2 = 2 + 0 \longrightarrow a_6 = 0$
$2/2 = 1 + 0 \longrightarrow a_7 = 0$
$1/2 = 1/2 \longrightarrow a_8 = 1$

$(a_8\ a_7\ a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0)_2$

$(1\ 0\ 0\ \ 0\ 0\ 0\ 0\ 1\ 1)_2$

$259_{10} = 100\ 00\ 00\ 11_2$

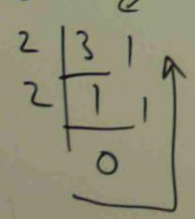
OCTAL

$$N_{10} = d_n 8^n + d_{n-1} 8^{n-1} + \cdots + d_2 8^2 + d_1 8^1 + d_0 8^0$$

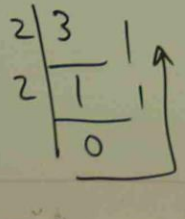
Pb FIND BINARY AND DECIMAL EQUIVALENT OF 33_8

OCTAL → BINARY

$33_8 =$ 3 & 3 →



$= 011$



$= 011$

$33_8 = 011\ 011_2$

OCTAL TO DECIMAL

$33_8 = 3 \times 8^1 + 3 \times 8^0$

$= 3 \times 8 + 3 \times 1$

$= 24 + 3 = 27_{10}$

$33_8 = 27_{10}$

HEX DECIMAL

$$N_{10} = C_n \times 16^n + C_{n-1} \times 16^{n-1} + \cdots C_2 \times 16^2 + C_1 \times 16^1 + C_0 \times 16^0$$

HEX DECIMAL NUMBERS

1H, 2H, 3H, 4H, 5H, 6H, 7H, 8H, 9H

10 ⟶ AH, 11 ⟶ BH, 12 ⟶ CH, 13 ⟶ DH, 14 ⟶ EH, 15 ⟶ FH

10 ⟶ A, 11 ⟶ B, 12 ⟶ C, 13 ⟶ D, 14 ⟶ E, 15 ⟶ F

Pb FIND THE DECIMAL EQUIVALENT OF 47H, 30DH AND A2FH

$$47H \longrightarrow 47 = 4 \times 16^1 + 7 \times 16^0 = 4 \times 16 + 7 \times 1 = 71_{10}$$

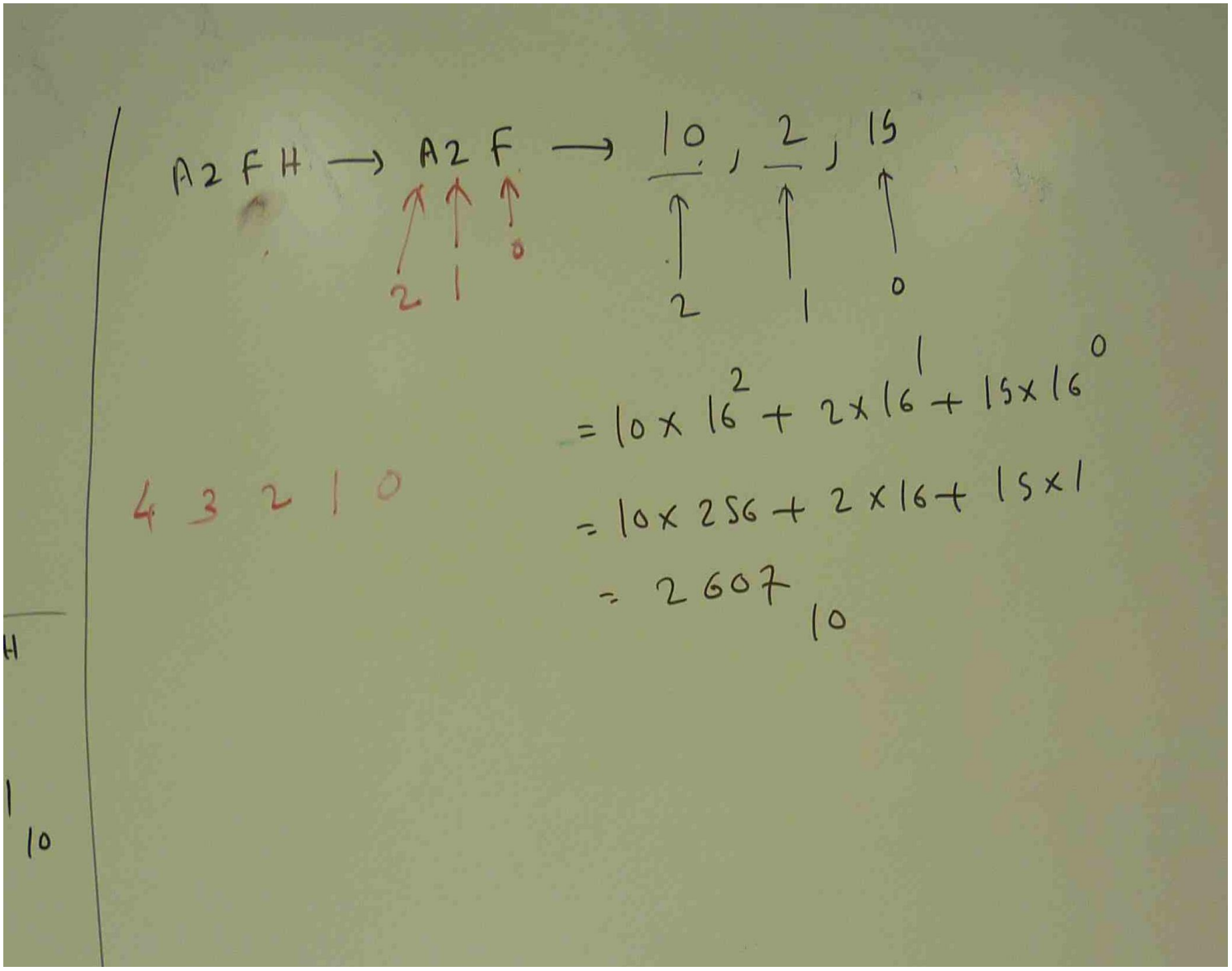
(1 0)

$$30DH \longrightarrow 30D = 3 \times 16^2 + 0 \times 16^1 + 13 \times 16^0$$

(2 1 0)

$$= 3 \times 256 + 0 \times 16 + 13 \times 1$$

$$= 781_{10}$$


A2FH → A2F → 10, 2, 15
2 1 0
2 1 0
4 3 2 1 0
= 10 × 16^2 + 2 × 16^1 + 15 × 16^0
= 10 × 256 + 2 × 16 + 15 × 1
= 2607_10

$+ C_{n-1} \times 16^{n-1} + \cdots C_2 \times 16^2 + C_1 \times 16^1 + C_0 \times 16^0$

BERS

H, 4H, 5H, 6H, 7H, 8H, 9H

11 → BH, 12 → CH, 13 → DH, 14 → EH, 15 → FH

11 → B 12 → C 13 → D 14 → E 15 → F

DECIMAL EQUIVALENT OF 47H, 30DH AND A2FH

$47 = 4 \times 16^1 + 7 \times 16^0 = 4 \times 16 + 7 \times 1 = 71_{10}$

$30D = 3 \times 16^2 + 0 \times 16^1 + 13 \times 16^0$

$= 3 \times 256 + 0 \times 16 + 13 \times 1$

$= 781_{10}$

HEX → DECIMAL $\times 16^n$

DECIMAL → HEXDECIMAL $\frac{}{16^n}$

$A2FH \rightarrow A2F \rightarrow 10, 2, 15$

2 1 0

4 3 2 1 0

$= 10 \times 16^2 + 2 \times 16^1 + 15 \times 16^0$

$= 10 \times 256 + 2 \times 16 + 15 \times 1$

$= 2607_{10}$

Pb FIND THE HEXDECIMAL EQUIVALENT OF 29_{10}

175_{10}, 3412_{10}

$29_{10} \rightarrow \frac{29}{16} = 1 + \frac{13}{16} = 1DH$

$175_{10} \rightarrow \frac{175}{16} = 10 + \frac{15}{16} = AFH$

10 ← RESULT

16 | 175

16

15 ← REMAINDER

$3412_{10} =$

16 | 3412

32

213

21

16

5

16 | 213

16

13

53

48

5

16 | 13

13

$A2FH \rightarrow A2F \rightarrow 10, 2, 15$

$= 10 \times 16^2 + 2 \times 16^1 + 15 \times 16^0$

$= 10 \times 256 + 2 \times 16 + 15 \times 1$

$= 2607_{10}$

4 3 2 1 0

Pb FIND THE HEXDECIMAL EQUIVALENT OF 29_{10}

175_{10}, 3412_{10}

$29_{10} \rightarrow \frac{29}{16} = 1 + \frac{13}{16} = 1D\,H$

$175_{10} \rightarrow \frac{175}{16} = 10 + \frac{15}{16} = AF\,H$

10 ← RESULT

16 | 175

16

15 ← REMAINDER

$3412_{10} = \frac{3412}{16} = 213 + \frac{4}{16} = 4$

213

16 | 3412

32

21

16

52

48

4

$\frac{213}{16} = 13 + \frac{5}{16} = 5$

13

16 | 213

16

53

48

5

$\frac{13}{16} = 0 + \frac{13}{16} = 13 = D$

16 | 13

13

$3412_{10} = D\,5\,4\,H$

NEGATIVE NUMBER

2's complement method is utilized to represent the negative numbers.

method (1) -1011_2 To be represented by 2's complement method

$$\begin{array}{r} 10000 \\ -\ 1011 \\ \hline 0101 \end{array}$$

← Two complement.

$-1011_2 = 0101_2$

method (2)

10000

1011 ←

same

0101 ⟶ 0101

add (1)

opposite

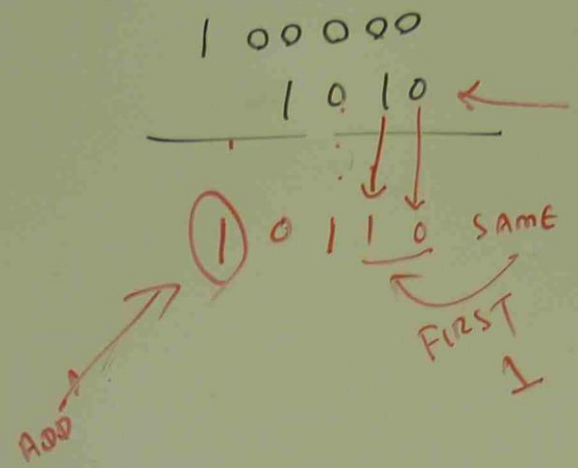
opposite

opposite

$-1011_2 = 0101_2$

2's complement

Ph $-1010_2 = ?$ 2's complement



$-1010_2 = 1011_2$

BEFORE REACHING THE FIRST 1 FROM RIGHT TO LEFT, JUST WRITE THE SAME NUMBER AFTER FIRST 1 THEN WRITE OPPOSITE NUMBERS.

FINALLY ADD 1 AT THE FRONT.

FRACTIONAL BINARY NUMBERS

$$N_{10} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_m 2^{-m}$$

N_{10} = BASE 10 NUMBER LESS THAN 1

FRACTIONAL BINARY TO DECIMAL CONVERSION

Ph FIND THE BASE 10 EQUIVALENT OF THE BINARY NUMBER 0.110101_2

$$N_{10} = 1\times 2^{-1} + 1\times 2^{-2} + 0\times 2^{-3} + 1\times 2^{-4} + 0\times 2^{-5}$$

$$= 1\times\frac{1}{2} + 1\times\frac{1}{2^2} + 0\times\frac{1}{2^3} + 1\times\frac{1}{2^4} + 0\times\frac{1}{2^5}$$

$$= \frac{1}{2} + \frac{1}{4} + 0 + \frac{1}{16} + 0$$

$$= 0.8125_{10}$$

FRACTIONAL DECIMAL TO BINARY OCTAL HEX DECIMAL

Pb FIND THE BINARY, OCTAL AND HEX DECIMAL EQUIVALENT of 0.3125_{10}

$0.3125_{10} \longrightarrow 2 \times 0.3125 = 0.6250 \longrightarrow b_1 = 0$

$2 \times 0.6250 = 1.250 \quad b_2 = 1$

(1.250 — LEFT)

$2 \times 0.250 = 0.500 \quad b_3 = 0$

$2 \times 0.500 = 1.0 \quad b_4 = 1$

FORMAT = $(0.b_1 b_2 b_3 b_4)_2 = (0.0101)_2$

$0.3125_{10} = 0.0101_2$ BINARY EQUIVALENT

TO CHANGE TO OCTAL

0.0101

3 BINARY BITS ARE TO BE COMBINED.

0.010100

3 BINARY BITS — PUT — 3 BINARY BIT

010 , 100 $= (24)_8$

2^2 PLACE, 2^1 PLACE, 2^0 PLACE

2^2 PLACE, 2^1 PLACE, 2^0 PLACE

$0\times2^2 + 1\times2^1 + 0\times2^0$

$0\times4 + 1\times2 + 0$

2

$1\times2^2 + 0\times2^1 + 0\times2^0$

$1\times4 + 0\times2 + 0\times1$

4

0.24_8 OCTAL EQUIVALENT

TO CHANGE TO HEX DECIMAL

0.0101

4 BINARY BITS ARE TO BE COMBINED

0.0101 0000

4 BINARY BIT

0101 , 0000

$2^3, 2^2, 2^1, 2^0$

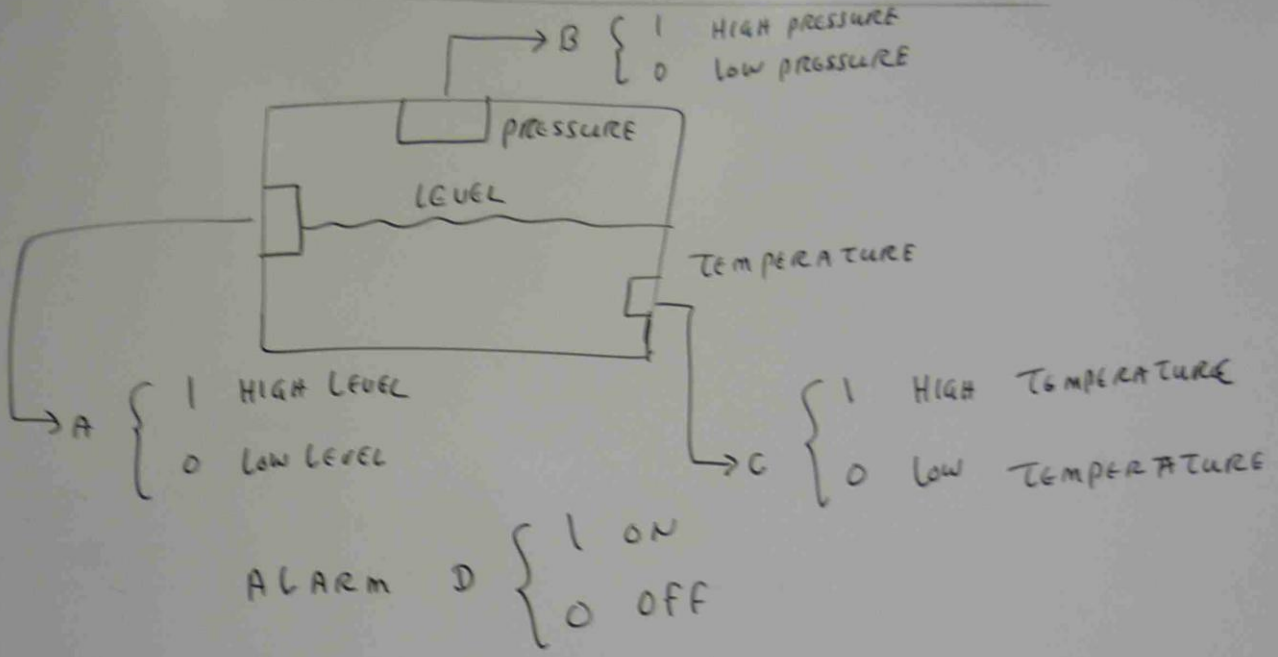
$0\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0$

$0 + 4 + 0 + 1 = 5$

$0\times2^3 + 0\times2^2 + 0\times2^1 + 0\times2^0 = 0$

0.50H

DESIGNING THE DIGITAL GATE SYSTEM TO CONTROL THE PROCESS



ALARM CONDITIONS ARE

1. LOW LEVEL WITH HIGH PRESSURE → ALARM SHOULD OPERATE
2. HIGH LEVEL WITH HIGH TEMPERATURE → ALARM SHOULD OPERATE
3. HIGH LEVEL WITH LOW TEMPERATURE AND HIGH PRESSURE → ALARM SHOULD OPERATE.

LEVEL (A)

LOW LEVEL = $\overline{A}$

HIGH LEVEL = A

PRESSURE (B)

LOW PRESSURE = $\overline{B}$

HIGH PRESSURE = B

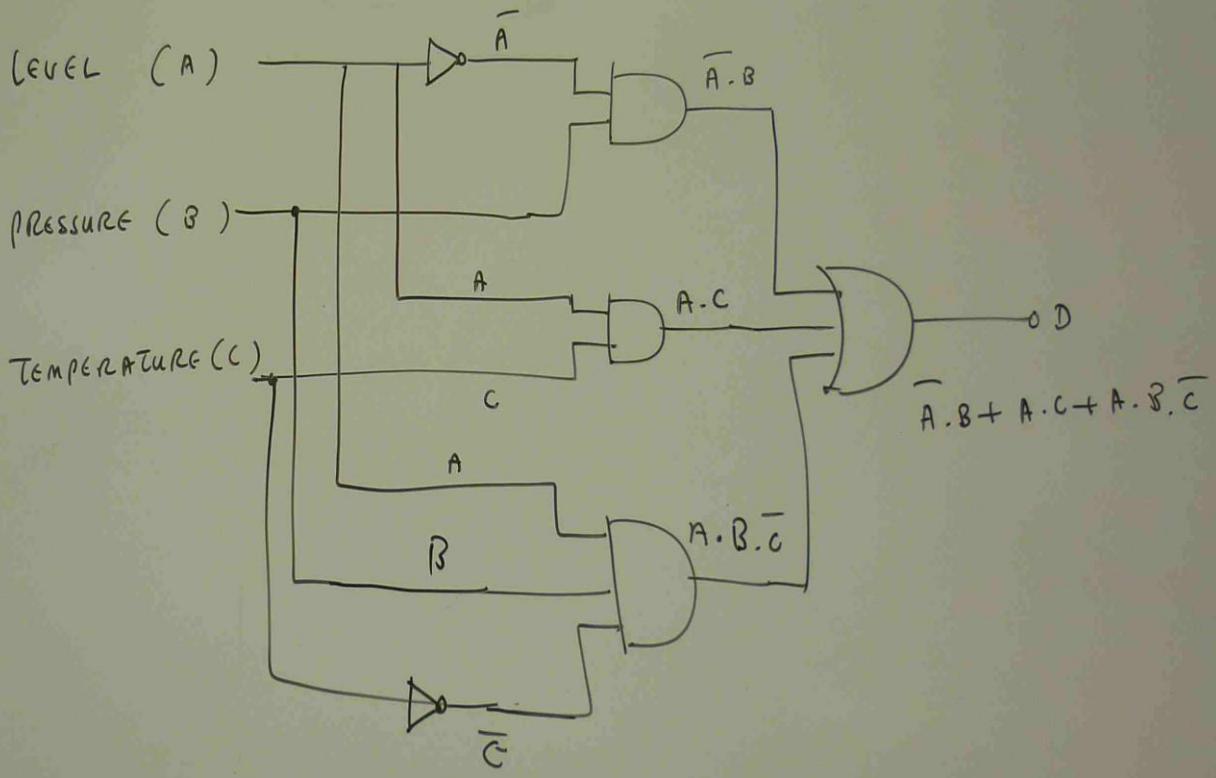
TEMPERATURE (C)

LOW TEMPERATURE = $\overline{C}$

HIGH TEMPERATURE = C

$$D = \overline{A}.B + A.C + A.B.\overline{C}$$

TO DEVELOP DIGITAL GATES



PROGRAMMABLE LOGIC CONTROLLERS

PLC ARE PARTICULARLY SUITED TO THE SOLUTION OF CONTROL PROBLEMS ASSOCIATED WITH BOOLEAN EQUATIONS AND BINARY LOGIC PROBLEMS IN GENERAL. THEY ARE A COMPUTER BASED OUT GROWTH OF RELAY SEQUENCE CONTROLLERS.

BUSES AND TRI STATE BUFFERS

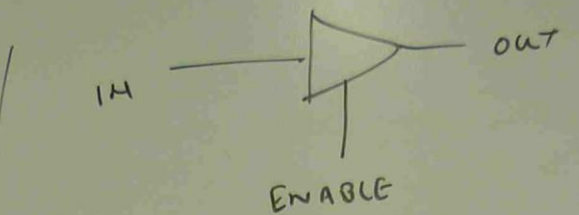
AN 8 BIT COMPUTER MAY HAVE A DATA BUS WITH 8 LINES IN PARALLEL. ALL DATA INPUT AND OUTPUT TO THE COMPUTER ARE CARRIED OVER THESE LINES.

TRI STATE BUFFERS

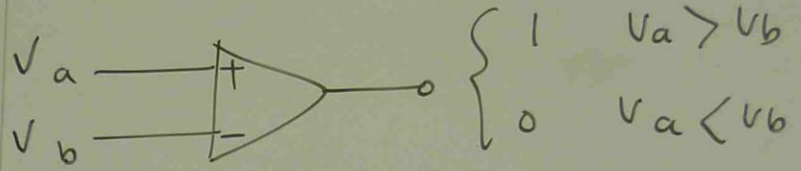
THIS IS A DEVICE THAT ACTS LIKE A SWITCH.

TRI STATE BUFFER HAS 3 STATES ON IT'S OUTPUT

LOGIC 1, LOGIC 0 HIGH IMPEDANCE (OPEN CIRCUIT)



COMPARATORS



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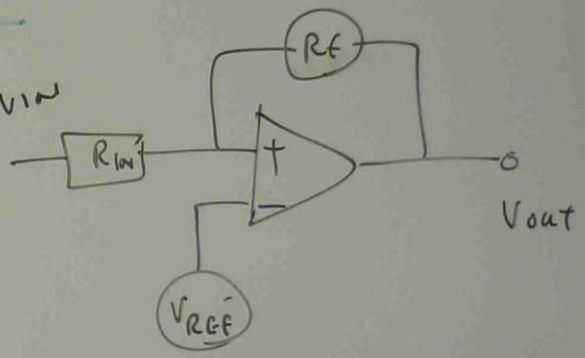
pb A PROCESS CONTROL SYSTEM SPECIFIES THAT TEMPERATURE SHOULD NEVER EXCEED 160°C IF THE PRESSURE ALSO EXCEEDS 10 Pa. DESIGN AN ALARM SYSTEM TO DETECT THIS CONDITION USING TEMPERATURE AND PRESSURE TRANSDUCERS WITH TRANSFER FUNCTION OF 2.2 mV/°C AND 0.2V/Pa RESPECTIVELY.

TEMPERATURE CONTROL
PRESSURE CONTROL
} HAPPENS AT THE SAME TIME → AND

COMPARATOR

INVERTING FUNCTION

NON INVERTING FUNCTION



TEMPERATURE

TEMPERATURE

160°C × 2.2mV/°C = 0.352 V

REF

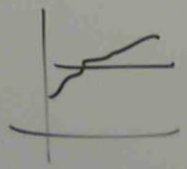
ALARM

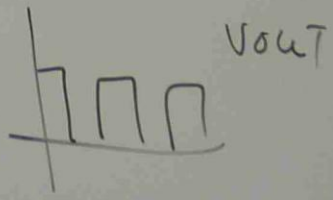
PRESSURE

0.2V/kPa × 10kPa → 2V

PRESSURE

$$V_{IN} = V_{REF} - \frac{R_{IN}}{R_{REF}} \times V_O$$





HYSTERESIS COMPARATOR

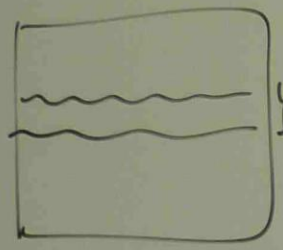
WHEN USING COMPARATOR, SWINING ABOUT THE REFERENCE LEVEL CAN CAUSE WRONG OPERATION.

SUCH PROBLEM CAN BE SOLVED BY PROVIDING DEAD BAND BY USING HYSTERESIS COMPARATOR

$$V_{IN} = V_{Ref} - \underbrace{\frac{R}{Rf} V_0}$$

DEAD BAND HYSTERESIS

Pb A TRANSDUCER CONVERTS THE LIQUID LEVEL IN A TANK TO VOLTAGE ACCORDING TO THE TRANSFER FUNCTION (20 mV/cm)
A COMPARATOR IS SUPPOSED TO GO HIGH (5V) WHENEVER THE LEVEL BECOMES 50 cm. SPLASHING CAUSES THE LEVEL TO FLUCTUATE BY ±3 cm. DEVELOP A HYSTERESIS COMPARATOR TO PROTECT AGAINST THE EFFECTS OF SPLASHING.



REF NOMINAL REFERENCE OCCURS AT 50cm

$$V_{Ref} = 50\,cm \times 20\,mV/cm = 1000\,mV = 1V$$

FLUCTUATION (±3cm)

NOISE

$$(\pm 3\,cm) \times 20\,mV/cm = \pm 60\,mV$$

– IN A TANK TO VOLTAGE

mV/cm)

V) WHENEVER THE LEVEL

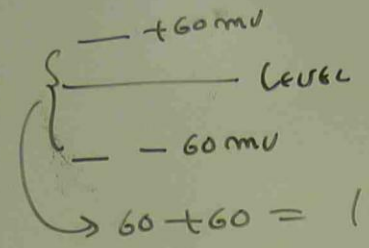
EL TO FLUCTUATE BY

PARATOR TO PROTECT

50cm

V/cm = 1000 mV = 1 V

mV/cm = ± 60 mV



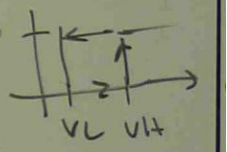
DEAD BAND VOLTAGE ⇒ $\frac{R}{Rf} \times V_{HIGH} =$ DEAD BAND VOLTAGE

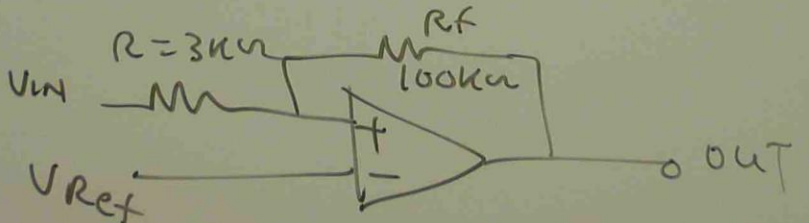
$\frac{R}{Rf} \times 5 = 150 \times 10^{-3}$

$\frac{R}{Rf} = \frac{150 \times 10^{-3}}{5} = 0.03$

IF $R_f = 100k\Omega$

$R = 0.03 \times 100k\Omega = 3k\Omega$





$V_L = V_{Ref} - \frac{R}{Rf} V_O$

$V_H = V_{Ref}$

DIGITAL TO ANALOG CONVERTERS (DACS)

$$V_{out} = V_R \left[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_m 2^{-m} \right]$$

BINARY

V_{out} = ANALOG OUTPUT VOLTAGE

V_R = REFERENCE VOLTAGE

$b_1, b_2 \cdots b_m$ = n BIT BINARY WORD

$$V_{out} = \frac{N}{2^n} \times V_{REF}$$

HEX

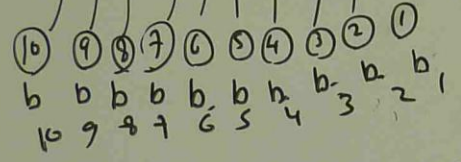
p6 WHAT IS THE OUTPUT VOLTAGE OF A 10 BIT ADC WITH A 10.0 V REFERENCE IF THE INPUT IS

(a) 001 0110 101 = 613 5H

(b) 20 FH ?

WHAT INPUT IS NEEDED TO GET A 6.5 V OUTPUT?

(a) 001 0110 101



$$V_{OUT} = V_R \left[b_1 2^{-1} + b_2 2^{-2} + \cdots b_m 2^{-m} \right]$$

$$= 10 \left[1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 0\times2^{-4} + 1\times2^{-5} + 1\times2^{-6} + 0\times2^{-7} + 1\times2^{-8} + 0\times2^{-9} + 0\times2^{-10} \right]$$

$$= 10 \times 0.176758$$

$$= 1.76758\ V$$

(b) 20FH

$2 \times 16^2 + 0 \times 16^1 + 15 \times 16^0 = 527_{10}$

$$V_{OUT} = \frac{N}{2^n} V_{REF}$$

$$= \frac{527}{2^{10}} \times 10 = 5.1464 V$$

FOR 6.5 V OUTPUT

$$V_{OUT} = \frac{N}{2^n} \times V_{REF}$$

$$6.5 = \frac{N}{2^{10}} \times 10 \rightarrow N = \frac{6.5 \times 2^{10}}{10} = 665.6 V$$

$$\Delta V_{OUT} = V_r \times 2^{-n}$$

ΔV_{OUT} = SMALLEST OUTPUT CHANGE

V_r = REFERENCE VOLTAGE

n = NUMBER OF BITS IN THE WORD

Ph CALCULATE ΔV_{OUT} FOR 5 BIT D/A CONVERTER WITH 10V REFERENCE.

$$\Delta V_{OUT} = V_r \times 2^{-n}$$

$$= 10 \times 2^{-5}$$

$$= \frac{10}{2^5}$$

$$= \frac{10}{32}$$

$$= 0.3125 \text{ V/BIT}$$

Ph DETERMINE HOW MANY BITS A D/A CONVERTER MUST HAVE TO PROVIDE OUTPUT INCREMENT OF 0.04 VOLT (OR) LESS. THE REFERENCE IS 10V.

ΔV = INCREMENT VOLTAGE $= V_r \times 2^{-n}$

$$0.04 = 10 \times 2^{-n}$$

$$\log 0.04 = \log 10 \times 2^{-n}$$

$$\log 0.04 = \log 10 + \log 2^{-n}$$

$$\log 0.04 = \log 10 + (-n)\log 2$$

$$\log 0.04 = 1 - n \log 2$$

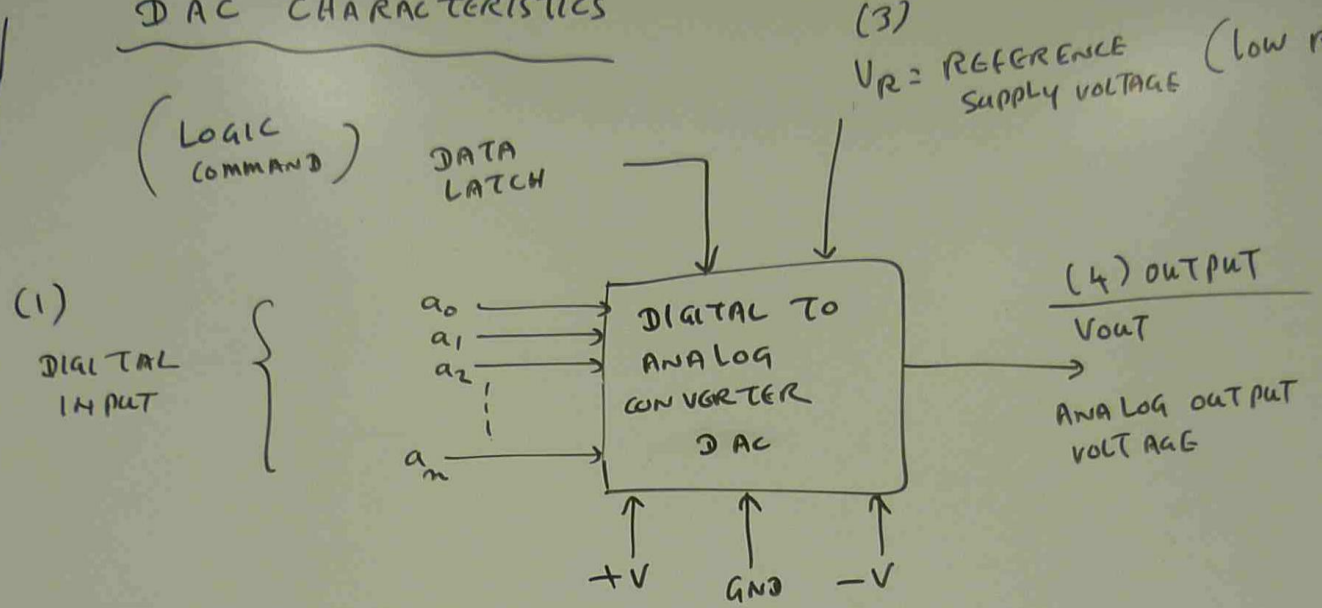
$$n \log 2 = 1 - \log 0.04$$

$$n = \frac{1 - \log 0.04}{\log 2} = 7.966 \simeq 8$$

BIT = 8 BIT

$$\Delta V_{OUT} = V_r \times 2^{-n} \rightarrow = 10 \times 2^{-8} = 0.03906 V$$

DAC CHARACTERISTICS



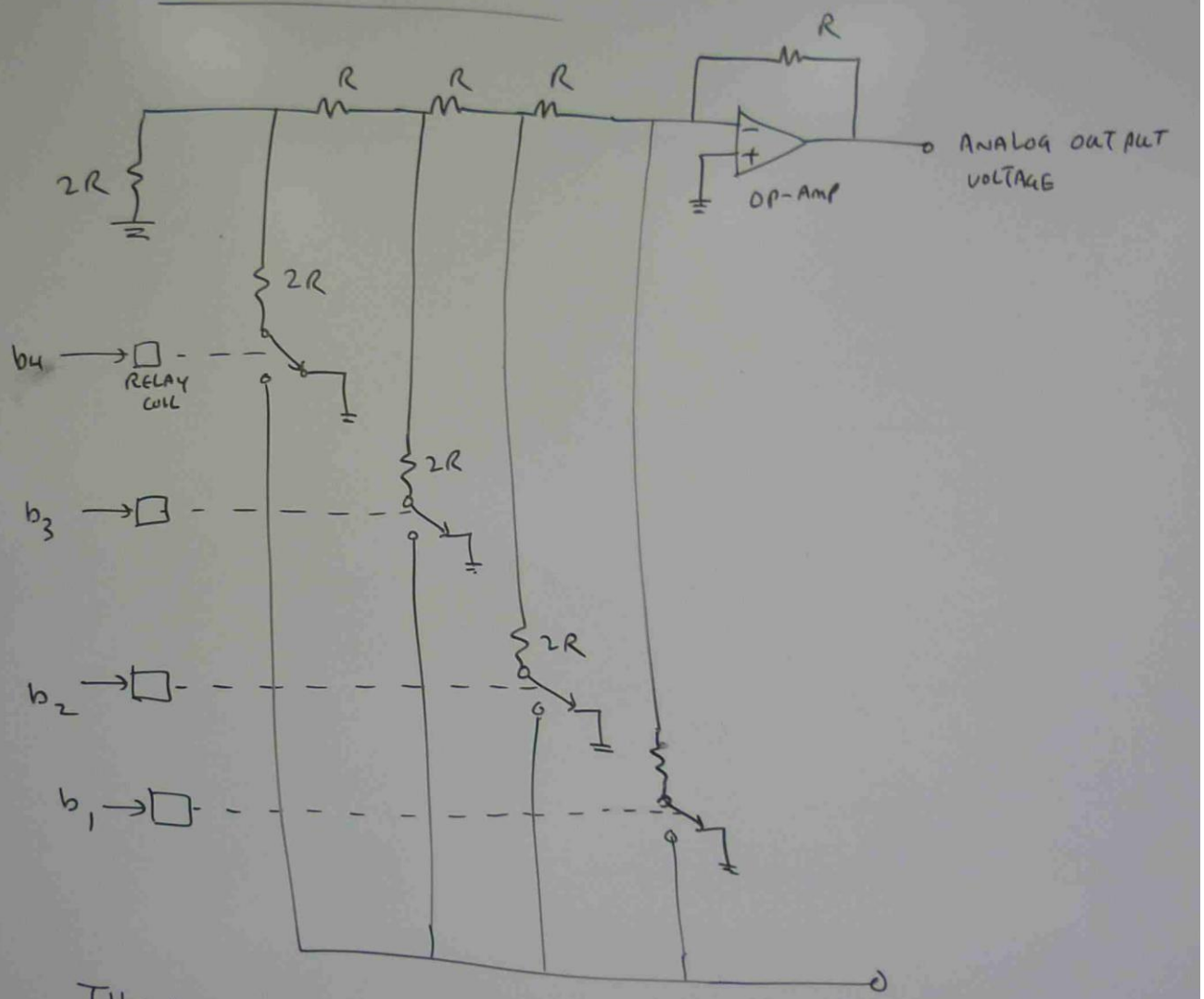
OFFSET

THE DAC IS USUALLY IMPLEMENTED WITH OP-AMP.

THERE MAY BE TYPICAL OUTPUT OFFSET VOLTAGE

WITH ZERO INPUT.

THE LADDER NETWORK



THE LADDER NETWORK IS OFTEN USED TO IMPLEMENT THE DAC FUNCTIONS.

P3 A CONTROL VALVE HAS A LINEAR VARIATION of OPENING AS THE INPUT VOLTAGE VARIES FROM 0 TO 10V.

A MICRO COMPUTER OUTPUTS AN 8 BIT WORD TO CONTROL VALVE OPENING USING AN 8 BIT DAC TO GENERATE THE VALVE VOLTAGE (a) FIND THE REFERENCE VOLTAGE REQUIRED TO OBTAIN A FULL OPEN VALVE (10V) (b) FIND THE PERCENTAGE OF VALVE OPENING FOR 1 BIT CHANGE IN THE INPUT WORD.

(a) FULL OPENING of VALVE, ALL 8 BITS ARE ONES.

$$V_{OUT} = V_{REF}\left[2^{-1} + 2^{-2} + 2^{-3} + \cdots 2^{-8}\right]$$

$$= 10\left[\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \cdots \frac{1}{2^8}\right]$$

$$= 10\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \cdots + \frac{1}{256}\right]$$

$$= 10.039V$$

IT NEEDS LARGER REF: VOLTAGE

(b) $\Delta V_{OUT} = V_R \times 2^{-n}$

1 BIT CHANGE

$\Delta V_{OUT} = 10.039 \times 2^{-8} = 0.0392V$

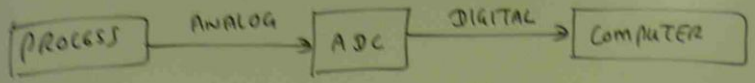
$\%\ CHANGE = \frac{\Delta V_{OUT}}{V_R} \times 100 = \frac{0.0392}{10} \times 100 = 0.392\%$

MICROPROCESSOR COMPATIBLE DAC

DATA OUTPUT BOARDS

ADDRESS DECODING, BUS INTERFACE, C, BASIC, ASSEMBLY.

ANALOG TO DIGITAL CONVERTER (ADC)



$$\Delta V = V_r \, 2^{-n}$$

$$V_{IN} = V_R \left[b_1 2^{-1} + b_2 2^{-2} + -- b_m 2^{-n} \right]$$

V_{IN} = ANALOG VOLTAGE INPUT

V_r = REFERENCE VOLTAGE

$b_1 \, b_2 - - b_n$ = N BIT.

Pb TEMPERATURE IS MEASURED BY A SENSOR WITH AN OUTPUT of 0.02 V/°C. DETERMINE THE REQUIRED ADC REFERENCE AND WORD SIZE TO TO MEASURE 0 → 100°C WITH 0.1°C RESOLUTION.

V_r = MAXIMUM TEMPERATURE °C × V/°C

$V_r = 100 \times 0.02 = 2\,V$ ←

ΔV = RESOLUTION × V/°C

$= 0.1 \times 0.02 = 0.002\,V$ ←

WORD SIZE = BIT = n = ?

$$\Delta V = V_r \times 2^{-n}$$

$$0.002 = 2 \times 2^{-n}$$

$$0.001 = 2^{-n}$$

$$\log 0.001 = \log 2^{-n}$$

$$\log 10^{-3} = -n \log 2$$

$$-3 \log 10 = -n \log 2$$

$$n = \frac{+3 \log 10}{+\log 2} = \frac{3 \times 1}{0.3010} \simeq 9.996 \simeq 10$$

10 BIT WORD IS REQUIRED FOR RESOLUTION.

$$\Delta V = V_r \times 2^{-n}$$

$$= 2 \times 2^{-10}$$

$$= 2^{-9} = \frac{1}{2^9} \simeq 0.00195\,V$$

Pb FIND THE DIGITAL WORD THAT RESULTS FROM A 3.127 V INPUT TO A 5 BIT ADC WITH A 5 VOLT REFERENCE.

THE RELATIONSHIP BETWEEN INPUT & OUTPUT

$$V_{IN} = V_r \left[a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + a_4 2^{-4} + a_5 2^{-5} \right]$$

$$3.127 = 5 \left[a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + a_4 2^{-4} + a_5 2^{-5} \right]$$

$$\frac{3.127}{5} = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + a_4 2^{-4} + a_5 2^{-5}$$

$$0.6254 = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + a_4 2^{-4} + a_5 2^{-5}$$

DIGITAL

$0.6254 \times 2 = 1.2508 \longrightarrow a_1 = 1$

$0.2508 \times 2 = 0.5016 \longrightarrow a_2 = 0$

$0.5016 \times 2 = 1.0032 \longrightarrow a_3 = 1$

$0.0032 \times 2 = 0.0064 \longrightarrow a_4 = 0$

$0.0064 \times 2 = 0.0128 \longrightarrow a_5 = 0$

$$(a_1 a_2 a_3 a_4 a_5)_2$$

OUTPUT $1\,0\,1\,0\,0_2$

Pb THE INPUT TO A 10 BIT ADC WITH A 2.5V REFERENCE IS 1.45V. WHAT IS THE HEX OUTPUT? SUPPOSE THE OUTPUT IS FOUND TO BE 1B4H. WHAT IS THE VOLTAGE INPUT?

1.45V

$$\text{INTEGER PART of ACTUAL OUTPUT (N BIT)} = \frac{V_{IN}}{V_r} \times 2^n$$

$$= \frac{1.45}{2.5} \times 2^{10}$$

$$= 593$$

16	593	1
16	37	5
	2	

$\longrightarrow$ 251H

1B4H

$1 \times 16^2 + 11 \times 16^1 + 4 \times 16^0$

$= 436\ V$

$$INT(N) = \frac{V_{IN}}{V_r} \times 2^n$$

$$436 = \frac{V_{IN}}{2.5} \times 2^{10}$$

$$V_{IN} = \frac{436 \times 2.5}{2^{10}}$$

$= 1.06445V$

BIPOLAR OPERATION

A BIPOLAR ADC IS THE ONE WHICH ACCEPTS INPUT BIPOLAR VOLTAGE FOR CONVERSION INTO AN APPROPRIATE DIGITAL OUTPUT.

THE NORMAL OUTPUT IS SHIFTED BY HALF, THE SCALE SO THAT ALL ZEROS CORRESPOND TO THE NEGATIVE MAXIMUM INPUT VOLTAGE INSTEAD OF ZERO

$$INT(N) = \frac{1}{UR}\left[V_{IN} + \frac{U_R}{2}\right] \times 2^n$$

By INCREASING ONE DIGITAL STEP, DECIMAL IS REPRESENTED.

pb REFERENCE VOLTAGE = 10 V, 8 BITS

IF −5 V IS REPRESENTED AT ALL BITS ZERO CONDITION, (REF)
DETERMING THE ONE STEP INCREMENT OF BIT.

$$\Delta V_{IN} = \frac{U_{REF}}{2^n} = \frac{10}{2^8} = 0.039\,V$$

$$-5\,V \longrightarrow 00000000$$

(1) STEP → $-5V + 0.039 = -4.961 \rightarrow 00000001_2$

ONE WHICH ACCEPTS INPUT BIPOLAR
TO AN APPROPRIATE DIGITAL OUTPUT.

FTED BY HALF, THE SCALE SO
D TO THE NEGATIVE MAXIMUM
OF ZERO

$$\left[V_{IN} + \frac{U_R}{2} \right] \times 2^n$$

E= 10V, 8 BITS

PRESENTED AT ALL BITS ZERO CONDITION, (REF)
NE STEP INCREMENT OF BIT.

$$= \frac{10}{2^8} = 0.039V$$

⟶ 00000000

$-4.961 \rightarrow 00000001_2$

BY INCREASING
ONE DIGITAL STEP,

DECIMAL IS
REPRESENTED.

$-5 + 0.039 \times 2 \rightarrow 00000010$

$-5 + 0.039 \times 3 \rightarrow 00000011$

$-5 + 0.039 \times 4 \rightarrow 00000100$

p11 WHAT IS THE HEX AND BINARY OUTPUT OF A BIPOLAR 8 BIT ADC WITH A 5 V REFERENCE FOR INPUTS OF −0.85 V AND +1.5 V? WHAT INPUT VOLTAGE WOULD CAUSE AN OUTPUT 72 H?

$$V_R = 5V \quad , \quad n = 8$$

$$INT(N) = \frac{1}{V_R}\left(V_{IN} + \frac{V_R}{2}\right) 2^n$$

$$= \frac{1}{5}\left(-0.85 + \frac{5}{2}\right) 2^8$$

$$= 84\ V$$

HEX

16 | 84 — 4 ↑ — 54H

$84_{10} \rightarrow$ HEX | 5

$84_{10} \rightarrow$ BINARY

2	84	0
2	42	0
2	21	1
2	10	0
2	5	1
2	2	0

8 BIT

$10\ 10\ 100 \rightarrow 0\ 1\ 0\ 10\ 100_2$

← 7 BIT →

← COMPARISON

OUTPUT 72 H

72 H →

↑ ↑

1 0 =

$$INT(N) = V_{IN} = \frac{1}{V_R}$$

$$114 = \frac{1}{5}$$

$V_{IN} = -$

→ PARALLEL FEED

com

V_{IN}

V_F

COMPARATOR COMP

INPUT VOLTAGE V

TO FEEDBACK

OLAR

of

ISE

OUTPUT 72 H

$72\,H \rightarrow 7\times16^{1} + 2\times16^{0}$

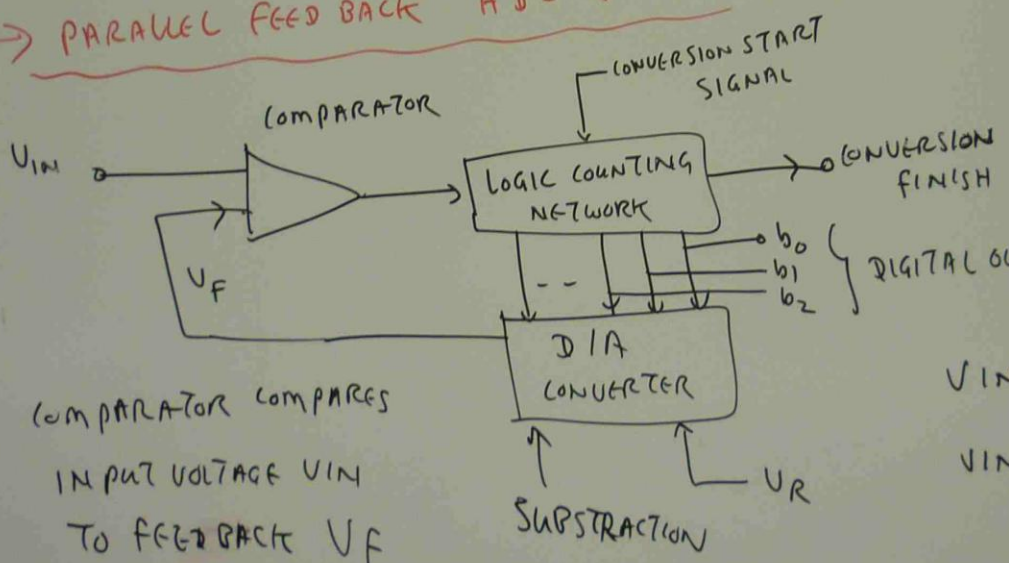
$= 114$ V

$$INT(N) = V_{IN} = \frac{1}{UR}\left(V_{IN} + \frac{UR}{2}\right)2^{n}$$

$$114 = \frac{1}{5}\left(V_{IN} + \frac{5}{2}\right)2^{8}$$

$V_{IN} = -0.2734$ V

PARALLEL FEED BACK ADC SYSTEM



COMPARATOR COMPARES INPUT VOLTAGE VIN TO FEEDBACK V_F.

b_1

$V_{IN} \begin{cases} V_R 2^{-1} \rightarrow \text{ZERO} \\ V_{IN} > U_R 2^{-2} \rightarrow b_2 = 1 \end{cases}$

$0\,|0|\,00_2$

Pb FIND THE SUCCESSIVE APPROXIMATION ADC OUTPUT FOR A 4 BIT CONVERTER TO A 3.217 V INPUT IF THE REFERENCE IS 5V.

INPUT = 3.217 V
REF = 5V

SET → N = 1

I $V_f = V_{ref} \times 2^{-n} = 5 \times 2^{-1} = \frac{5}{2} = 2.5V$

$V_{IN} = 3.217V$, $V_f = 2.5V$

$V_{IN} > V_f \longrightarrow b_1 = 1$

II INPUT = 3.217V, SET $n = 2$

REF = 5V

$V_f = \left(V_{ref} \times 2^{-n} + \frac{V_{ref}}{2}\right) = 5 \times 2^{-2} + \frac{5}{2} = 3.75V$

COMPARE V_{IN} 3.217 V WITH V_f 3.75V

$V_f > V_{IN} \longrightarrow b_2 = 0$

III INPUT =
REF =

COMPA

IV INPUT
REF

III INPUT = 3.217 V SET $n=3$

Ref = 5V $\longrightarrow$ $V_f = V_{ref} \times 2^{-n} + \frac{V_{ref}}{2}$

$= 5 \times 2^{-3} + \frac{5}{2} = 3.125\,V$

b_1	b_2	b_3	b_4
1	0	1	0

$_2$

COMPARE V_{IN} 3.217 V WITH V_f 3.125V

$V_{IN} > V_f \longrightarrow b_3 = 1$

IV INPUT = 3.217V SET $n=4$

Ref = 5V

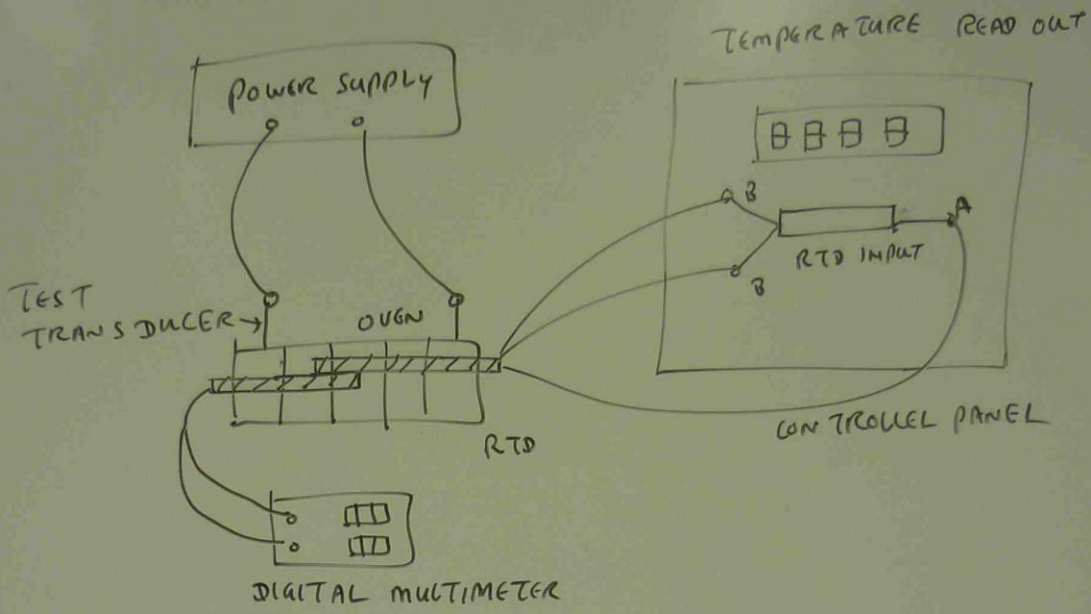
$V_f = V_{ref} \times 2^{-n} + \frac{V_{ref}}{2}$

$= 5 \times 2^{-4} + \frac{5}{2} = 3.437\,V$

COMPARE V_{IN} 3.217 V WITH V_f 3.437V

$V_f > V_{IN} \longrightarrow b_4 = 0$

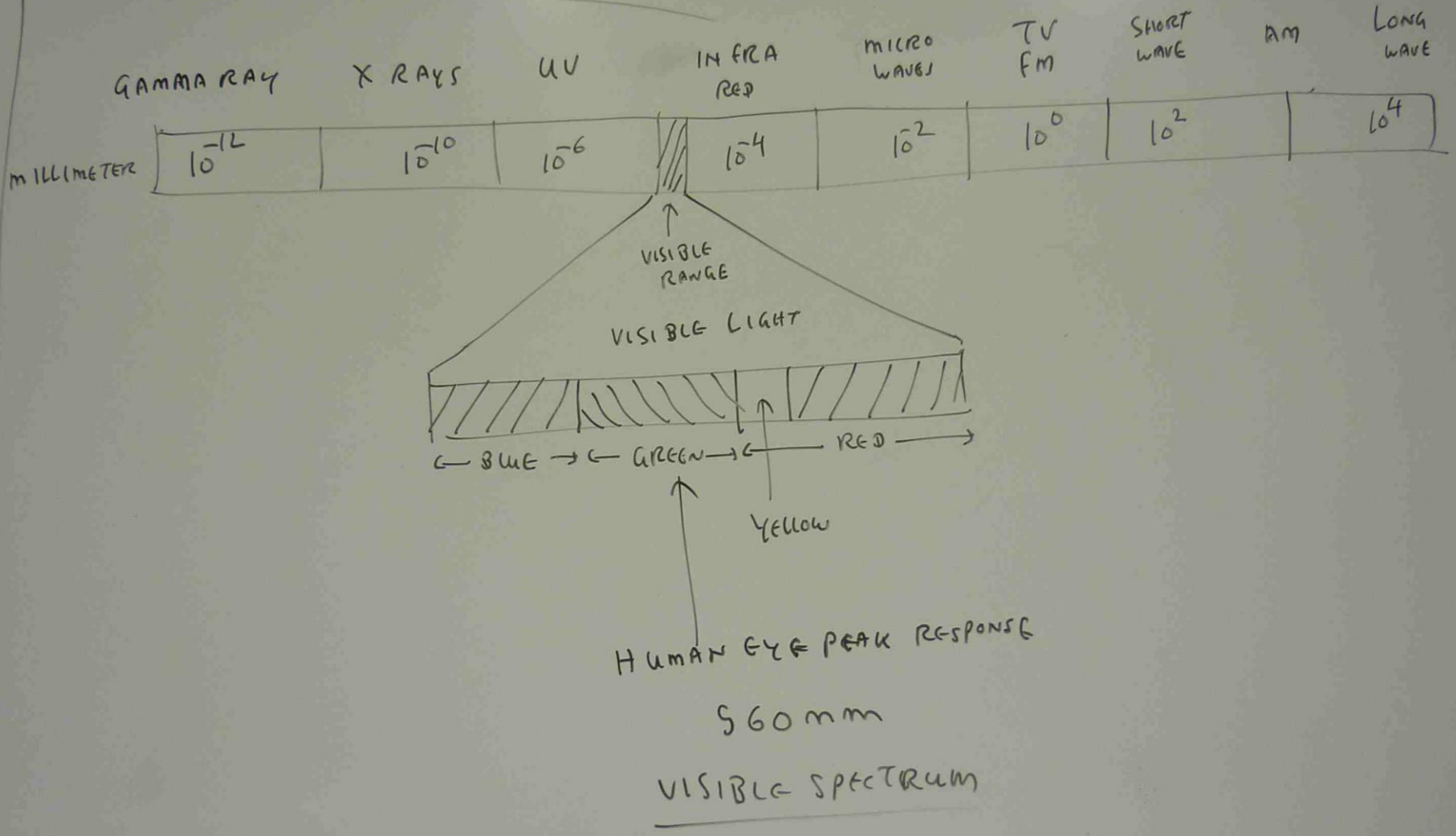
TEMPERATURE MEASUREMENT



EQUIPMENT

- TEMPERATURE TRANSDUCER (RTD, THERMISTOR, THERMOCOUPLE)
- DIGITAL MULTIMETER
- HEATING OVEN
- UNIVERSAL CONNECTING BLOCK
- DC POWER SUPPLY - 2A
- TEMPERATURE CONTROL PANEL
- CONNECTION LEAD - 4mm BANANA LEAD

LIGHT AND LIGHT TRANSDUCERS



AM LONG WAVE

10^4

LDR (LIGHT DEPENDENT RESISTOR) → PHOTO CONDUCTIVE CELL

(0.6ϕ × 15mm)

OPERATION

LIGHT FALLING ON THE SURFACE OF LDR CAUSES A DECREASE IN RESISTANCE THAT IS PROPORTIONAL TO THE AMOUNT OF LIGHT

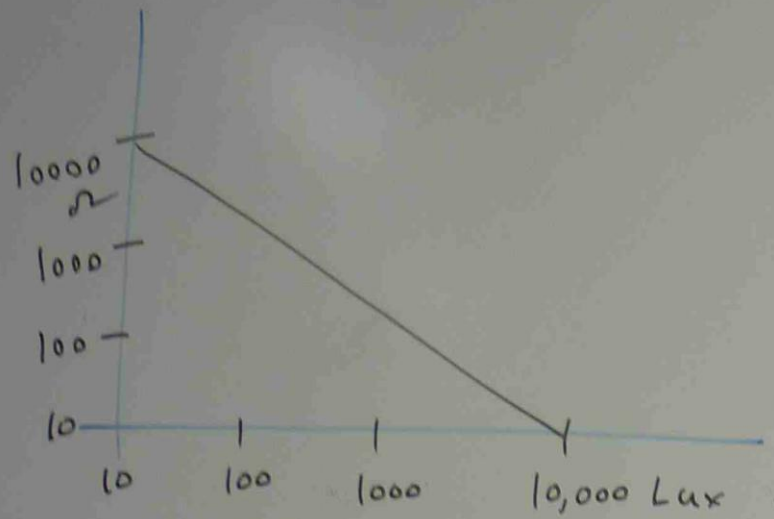
DARK VALUE R_D = MINIMUM 10MΩ (TOTAL DARKNESS)

LIGHT VALUE R_L = 75 – 300Ω (MEASURED AT 1000 LUX)

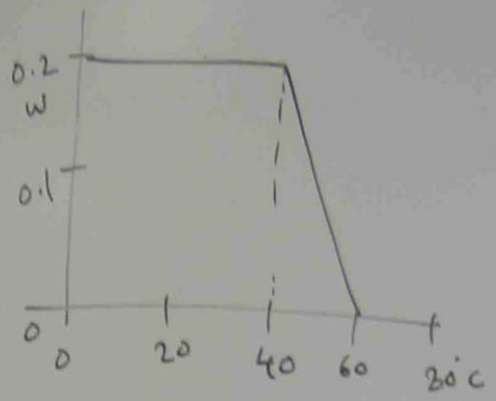
PERMISSIBLE VOLTAGE = E_{MAX} = 150V

AMBIENT TEMPERATURE = −20 → +60°C

CAPACITANCE 6 pf



RESISTANCE VALUE AS FUNCTION OF LIGHT INTENSITY



DERATING CURVE

Two Types of LDRs ARE AVAILABLE AND THEIR RESPONSES ARE AS Follows

CADMIUM SELENIDE Cdse = 735nm (INFRARED)

CADMIUM SULPHIDE CdS = 530nm To 600 nm (EYE)

DIGITAL TO ANALOG CONVERTORS (DACS)

$$V_{out} = V_R \left[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_m 2^{-m} \right]$$

V_{out} = ANALOG OUTPUT VOLTAGE

V_R = REFERENCE VOLTAGE

$b_1, b_2 \cdots b_m$ = n BIT BINARY WORD

$$V_{out} = \frac{N}{2^n} V_{ref}$$

Pb WHAT IS THE OUTPUT VOLTAGE OF A 10 BIT DAC WITH A 10 V REFERENCE IF THE INPUT IS (a) 001 0110101

(b) 20FH

WHAT INPUT IS NEEDED FOR 6.5 V OUTPUT

(a) $V_{OUT} = V_{REF}\left(b_1 2^{-1} + b_2 2^{-2} + - - - b_n 2^{-n} \right]$

$= 10\ (0\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3} + 0\times 2^{-4} + 1\times 2^{-5} + 1\times 2^{-6} + 0\times 2^{-7} + 1\times 2^{-8} + 0\times 2^{-9} + 1\times 2^{-10}]$

$= 10 \times 0.1767$

$= 1.767$ VOLT

(b) $20FH = 2\times 16^2 + 0\times 16^1 + 15\times 16^0 = 527_{10}$

$\uparrow\uparrow\uparrow$
$2\ 1\ 0$

$$V_{OUT} = \frac{N}{2^n} V_{ref} = \frac{527}{2^{10}} \times 10 = 5.14648\ V$$

$$V_{OUT} = \frac{N}{2^n} V_{ref}$$

$$6.5 = \frac{N}{2^{10}} \times 10$$

$$N = \frac{6.5 \times 2^{10}}{10} = 665.6\ V$$

$$\Delta V_{OUT} = V_r \times 2^{-n}$$

ΔV_{OUT} = SMALLEST OUTPUT CHANGE

V_r = REFERENCE VOLTAGE

n = NUMBER OF BITS IN THE WORD.

pb 5 BIT D/A CONVERTER, 10V REFERENCE

$$\Delta V_{OUT} = V_r \times 2^{-n}$$

$$\Delta V_{OUT} = 10 \times 2^{-5} = 0.3125 \text{ V/BIT}$$

Pb FIND THE SUCCESSIVE APPROXIMATION ADC OUTPUT FOR A 4 BIT CONVERTER TO A 3.217 V INPUT IF THE REFERENCE IS 5V.

(V_{IN}) I/P = 3.217 V SET n = 1

REF = 5 V

$$V_f = V_{REF} \times 2^{-n} = 5 \times 2^{-1} = \frac{5}{2} = 2.5V$$

V_{IN} COMPARES WITH V_f

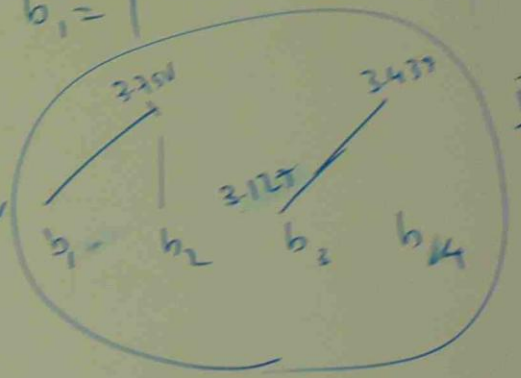
$V_{IN} > V_f$ (3.217 > 2.5) $\longrightarrow b_1 = 1$

II SET n = 2

$$V_f = V_{ref} \times 2^{-n} + \frac{V_{ref}}{2}$$

$$= 5 \times 2^{-2} + \frac{5}{2}$$

$$= 3.75V$$



V_{IN} COMPARES WITH V_f (3.217 < 3.75) $\longrightarrow b_2 = 0$

III SET $n = 3$

$$V_f = V_{ref} \times 2^{-n} + \frac{V_{ref}}{2}$$

$$= 5 \times 2^{-3} + \frac{5}{2}$$

$$= 3.127\ V$$

V_{IN} COMPARES WITH V_f $\quad V_{IN} > V_f \longrightarrow b_3 = 1$

3.217 3.127

IV SET $n = 4$

$$V_f = V_{REF} \times 2^{-n} + \frac{V_{REF}}{2}$$

$$= 5 \times 2^{-4} + \frac{5}{2}$$

$$= 3.437\ V$$

V_{IN} COMPARES WITH V_f $\quad V_{IN} < V_f \longrightarrow b_4 = 0$

3.217 3.437

b_1	b_2	b_3	b_4
1	0	1	0

RAMP A/D (RAMP ANALOG TO DIGITAL CONVERTER)

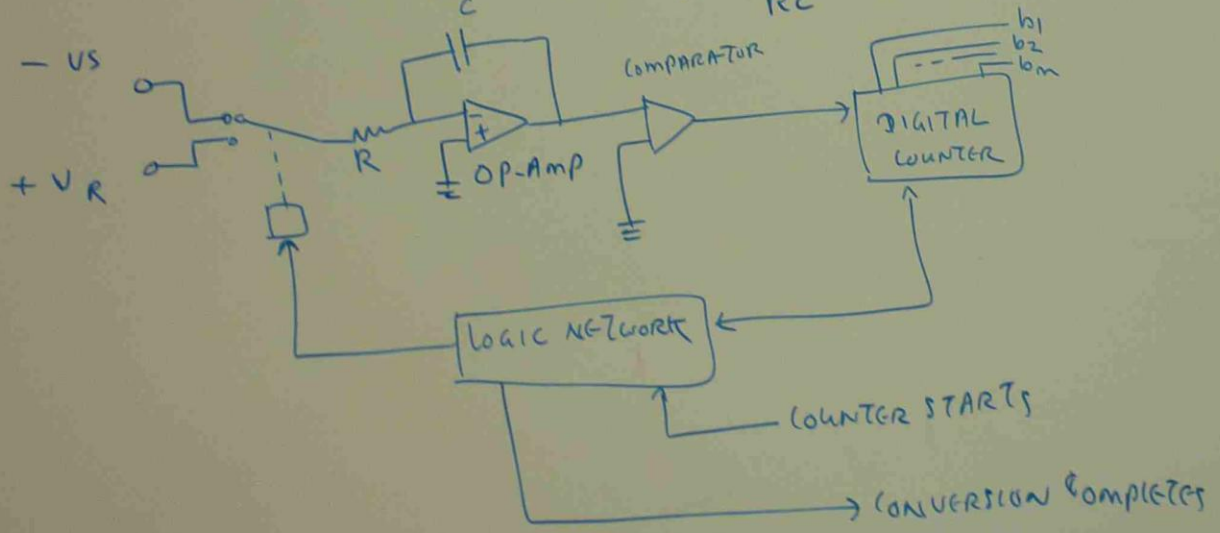
THE RAMP TYPE A/D CONVERTERS ESSENTIALLY COMPARE THE INPUT VOLTAGE AGAINST A LINEARLY INCREASING RAMP VOLTAGE.

DUAL SLOPE A/D

THE INPUT SIGNAL TO DRIVE THE INTEGRATOR FOR A FIXED TIME (T_1)

GENERATING OUTPUT $V_1 = \frac{1}{RC} \int V_x \, dt$

$$V_1 = \frac{1}{RC} T_1 V_x$$



A DUAL SLOPE ADC WAS AN OP-AMP INTEGRATOR, COMPARATOR AND ASSOCIATED DIGITAL CIRCUITS.

DIGITAL TO ANALOG CONVERTERS (DACS)

$$V_{out} = V_R \left[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_m 2^{-m} \right]$$

V_{out} = ANALOG OUTPUT VOLTAGE

V_R = REFERENCE VOLTAGE

$b_1, b_2 \cdots b_m$ = n BIT BINARY WORD

$$V_{out} = \frac{N}{2^n} V_{ref}$$

Pb WHAT IS THE OUTPUT VOLTAGE OF A 10 BIT DAC WITH A 10V REFERENCE IF THE INPUT IS (a) 0010110101

(b) 20FH

(c) WHAT INPUT IS NEEDED FOR 6.5 V OUTPUT

(a) $V_{out} = V_{REF}\left(b_1 2^{-1} + b_2 2^{-2} + \cdots b_m 2^{-m} \right)$

$= 10 \left(0\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 0\times2^{-4} + 1\times2^{-5} + 1\times2^{-6} + 0\times2^{-7} + 1\times2^{-8} + 0\times2^{-9} + 1\times2^{-10}\right]$

$= 10 \times 0.1767$

$= 1.767$ VOLT

(b) $20FH = 2\times16^2 + 0\times16^1 + 15\times16^0 = 527_{10}$

(2 1 0)

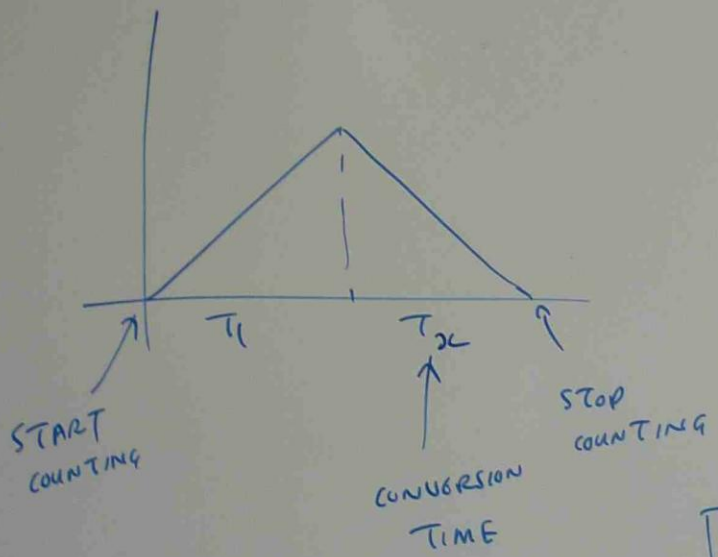
$$V_{out} = \frac{N}{2^n} V_{ref} = \frac{527}{2^{10}} \times 10 = 5.14648\ V$$

(c) $V_{out} = \frac{N}{2^n} V_{ref}$

$$6.5 = \frac{N}{2^{10}} \times 10$$

$$N = \frac{6.5 \times 2^{10}}{10} = 665.6 \simeq 665_{10}$$

Pb A DUAL SLOPE ADC AS SHOWN IN FIGURE HAS $R = 100\ k\Omega$, $C = 0.01\ \mu F$. THE REFERENCE IS 10 V AND THE FIXED INTEGRATION TIME IS 10 ms. FIND THE CONVERSION TIME FOR 6.8 V INPUT.



$$V_1 = \frac{1}{RC} T_1 V_x$$

$$V_1 = \frac{1}{100\times10^{3} \times 0.01\times10^{-6}} \times 10\times10^{-3} \times 6.8$$

$$V_1 = 6.8\ V$$

$$T_x = \text{CONVERSION TIME} = \frac{T_1 \times V_1}{V_R}$$

$$= \frac{10\times10^{-3} \times 6.8}{10}$$

$$= 6.8\ ms$$

GENERAL CHARACTERISTICS

(1) INPUT — COMMON LEVEL $0 \rightarrow 10$, $0 \rightarrow 5$ V, $-10 \rightarrow +10$ V

(2) OUTPUT

A PARALLEL (OR) SERIAL BINARY WORD THAT IS ENCODING OF THE ANALOG INPUT

(3) REFERENCE

A STABLE, LOW RIPPLE SOURCE AGAINST WHICH THE CONVERSION IS PERFORMED

(4) POWER SUPPLY

GENERALLY A BIPOLAR ± 12 V TO ± 18 V SUPPLY IS REQUIRED FOR THE ANALOG AMPLIFIERS AND COMPARATORS AND a $+5$ V SUPPLY FOR DIGITAL CIRCUITRY

(5) DIGITAL SIGNAL

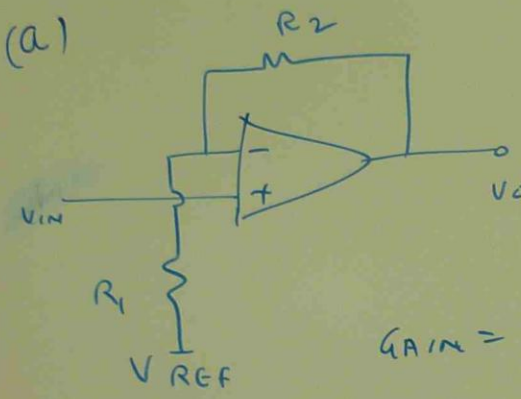
THE ADC USUALLY PROVIDES A HIGH LEVEL ON ANOTHER LINE AS AN INDICATOR.

P5

A MEASUREMENT OF TEMPERATURE USING A SENSOR THAT OUTPUTS 6.5 mV/°C MUST MEASURE TO 100°C. A 6 BIT ADC WITH A 10 V REFERENCE IS USED (a) DEVELOP AC CIRCUIT TO INTERFACE WITH THE SENSOR AND ADC

(b) FIND THE TEMPERATURE RESOLUTION.

(a)



$$GAIN = \frac{RF}{R1}$$

$$GAIN = \frac{V_{OUT}}{V_{IN}}$$

$V_{IN} = V/°C \times$ TEMPERATURE MEASURE

$= 6.5 \times 10^{-3} \times 100$

$= 0.65\ V$

$V_{OUT} = V_R (a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \cdots a_6 2^{-6})$

$a_1 = 1,\ a_2 = 1,\ a_3 = 1 \cdots a_6 = 1$

$V_{OUT} = V_R (1 \times 2^{-1} + 1 \times 2^{-2} + \cdots 1 \times 2^{-6})$

$= 10\left(\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} + \frac{1}{2^5} + \frac{1}{2^6}\right)$

$= 9.84375\ V$

$$GAIN = \frac{V_{OUT}}{V_{IN}} = \frac{9.84375}{0.65} = 15.14$$

$$GAIN = \frac{R_F}{R_1}$$

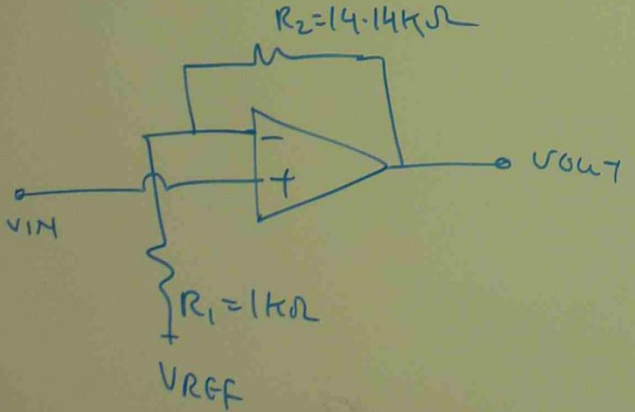
$$R_F = R_1 + R_2$$

$$15.14 = R_1 + R_2$$

SET $R_1 = 1k\Omega$

$$15.14 = 1 + R_2$$

$$R_2 = 14.14k\Omega$$



(b)

TEMPERATURE RESOLUTION

$$\Delta T = \frac{\Delta V_T}{V/^\circ C}$$

$V/^\circ C = 6.5\ mV/^\circ C$

$\Delta V_T = ?$

$$\Delta V_T = \frac{\Delta V}{GAIN}$$

$$\Delta V = V_R \times 2^{-n}$$

$$\Delta V = V_R \times 2^{-n}$$

$$\Delta V = 10 \times 2^{-6}$$

$$= 0.15625V$$

15.14 (b)

TEMPERATURE RESOLUTION

$$\Delta T = \frac{\Delta V_T}{V/^{\circ}C}$$

$V/^{\circ}C = 6.5\ mV/^{\circ}C$

$\Delta V_T = ?$

$$\Delta V_T = \frac{\Delta V}{GAIN}$$

$$\Delta V = V_R \times 2^{-n}$$

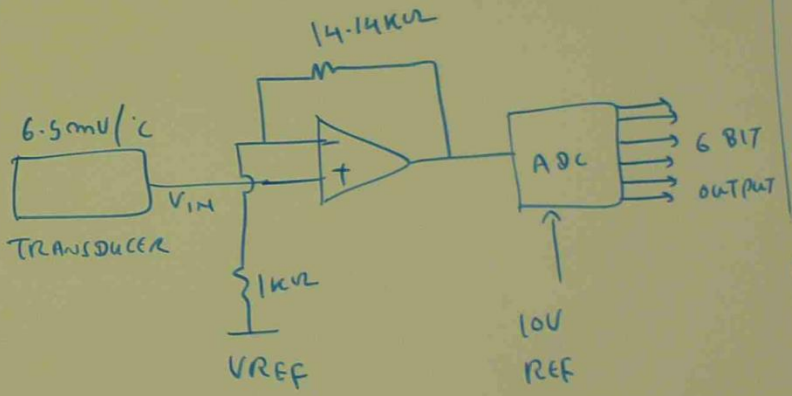
$$\Delta V = V_R \times 2^{-n}$$

$$\Delta V = 10 \times 2^{-6}$$

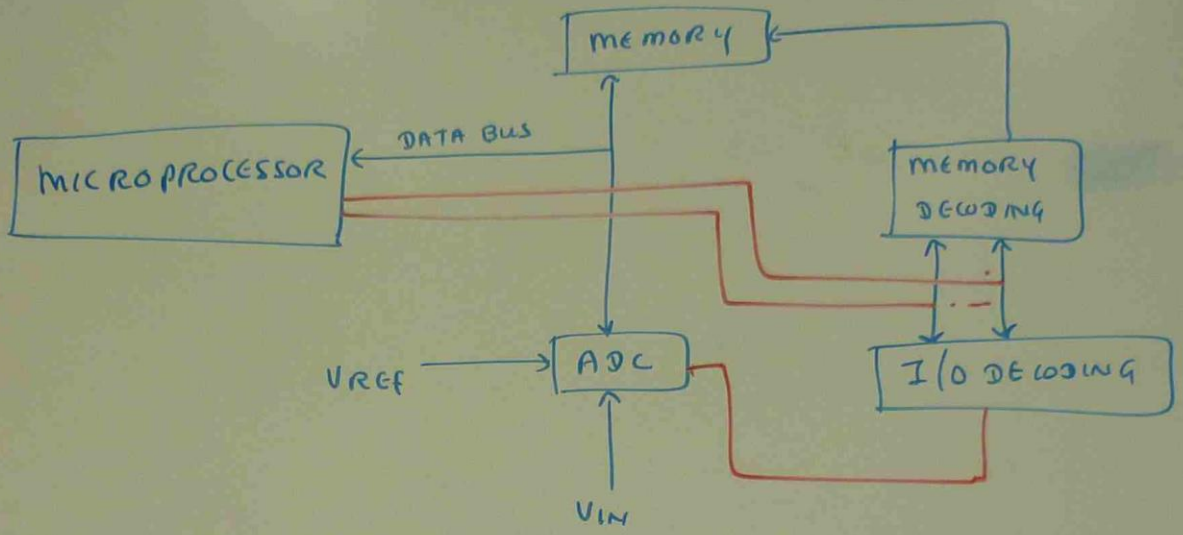
$$= 0.15625\,V$$

$$\Delta V_T = \frac{\Delta V}{GAIN} = \frac{0.15625}{15.14} = 0.01012\,V$$

$$\Delta T = \frac{\Delta V_T}{V/^{\circ}C} = \frac{0.01012}{6.5 \times 10^{-3}} = 1.59^{\circ}C$$



MICROPROCESSOR COMPATIBLE ADC



A WHOLE LINE of ADC HAVE BEEN DEVELOPED THAT INTERFACE EASILY WITH MICROPROCESSOR BASED COMPUTERS.

THE ADCs HAVE BUILT IN TRISTATE OUTPUTS SO THAT THEY CAN BE CONNECTED DIRECTLY TO DATA BUS of COMPUTER.

DATA FROM ADC IS ONLY PLACED ON DATA BUS LINES WHEN THE COMPUTER ISSUES AN APPROPRIATE ENABLE COMMAND (READ).

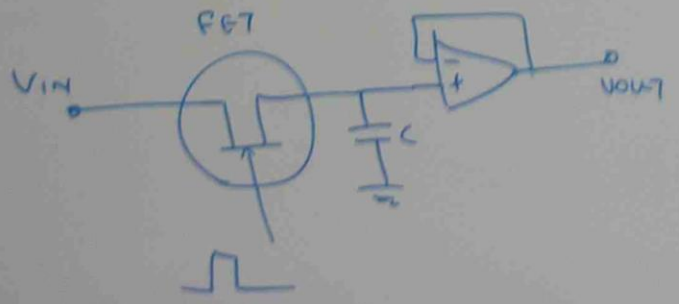
DATA INPUT BOARD

DATA INPUT BOARD, ADDRESSING, DECODING, BUS INTERFACE REFERENCE FOR CONVERTERS.

SAMPLE AND HOLD

THE ADC REQUIRES A CERTAIN LENGTH OF TIME TO DETERMINE THE APPROPRIATE DIGITAL OUTPUT FROM AN ANALOG INPUT (TIME A FEW μs → ms)

DURING CONVERSION — IT IS NECESSARY TO FREEZE THE INPUT SIGNAL. THIS CAN BE DONE USING A SPECIAL OP-AMP CIRCUIT CALLED SAMPLE & HOLD



WHEN THE FET IS DRIVEN TO THE ('OPEN') STATE, THE VOLTAGE ON THE CAPACITOR WILL HOLD THE LAST VALUE BEFORE OPEN STATE OF FET OCCURS.

DATA ACQUISITION SYSTEM

COMPUTER CONTROLS MANY VARIABLES.

COMPUTER PERIODICALLY SAMPLES THE VALUE OF A VARIABLE.

EVALUATE IT ACCORDING TO PROGRAMMED CONTROL

OPERATIONS AND OUTPUTS AN APPROPRIATE CONTROLLING

SIGNAL TO THE FINAL CONTROL ELEMENT

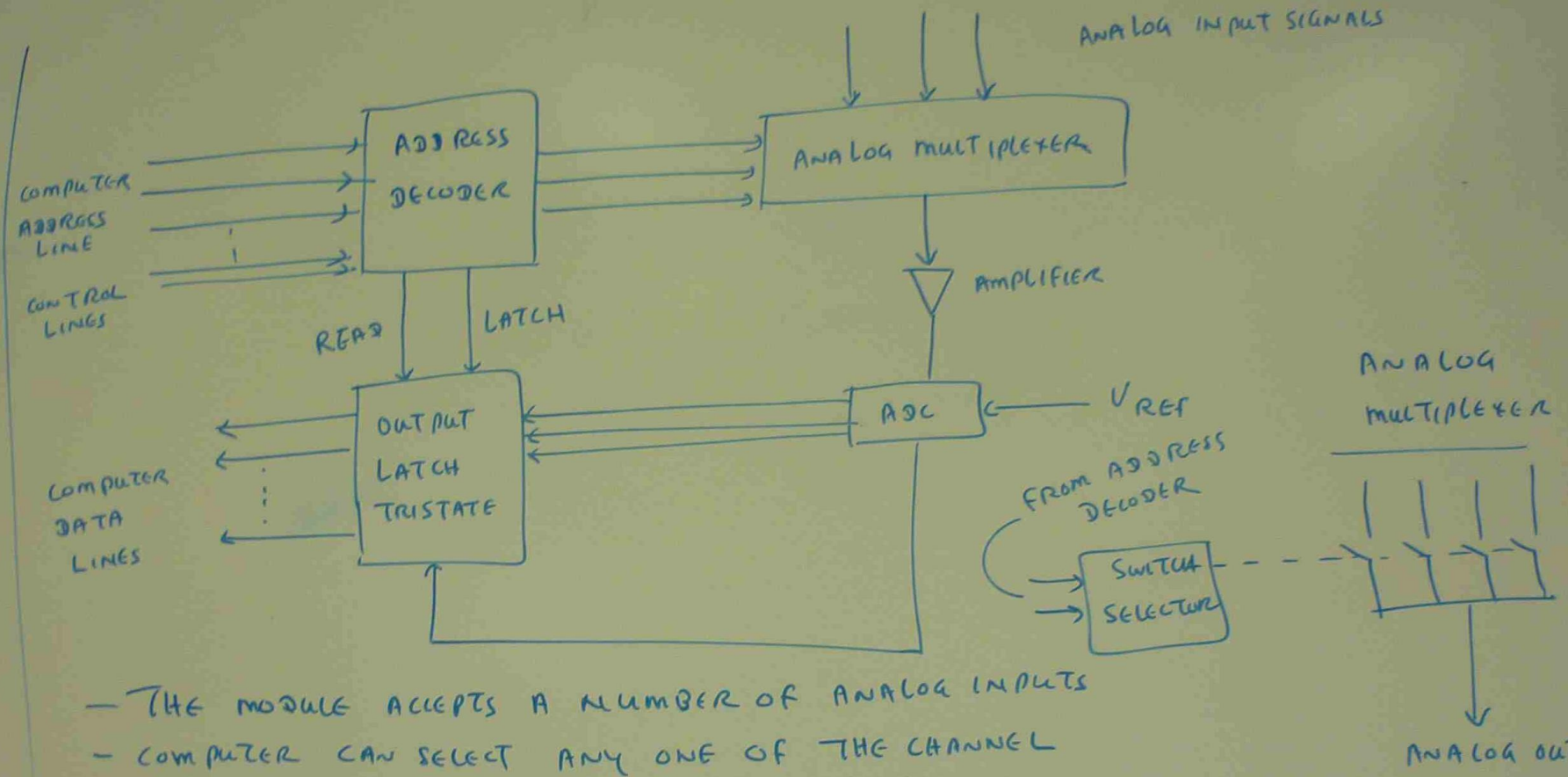
(SAMPLE | EVALUATE (OUTPUT)

INTERFACE

NECESSARY AMPLIFIERS & WRITE THE PROGRAMS

REQUIRED TO PUT TOGETHER AN INTERFACE

TO SOME COMPUTERS FOR A PROCESS APPLICATION.



- THE MODULE ACCEPTS A NUMBER OF ANALOG INPUTS
- COMPUTER CAN SELECT ANY ONE OF THE CHANNEL UNDER PROGRAM CONTROL FOR INPUT DATA

- DAS (DATA ACQUISITION SYSTEM) ACCEPTS THE INPUT FROM THE COMPUTER VIA ADDRESS LINES.

AMPLIFIER

VARIABLE GAIN AMPLIFIER

ADC

THE ADC CONVERTER ACCEPTS THE VOLTAGES THAT SPAN A SPECIFIC RANGE AS PROVIDED BY THE PRECEEDING SIGNAL CONDITIONING

SAMPLE & HOLD

HOLD THE VALUE DURING THE CONVERSION.

HARDWARE PROGRAMMING

ADDRESS SELECTION, AMPLIFIER GAIN, DIFFERENTIAL SINGLE-ENDED OPERATION.

SELECT BY JUMPERS / PINS.

SOFTWARE PROGRAMMING

USE DATA MODULES.

ADVANCED CERTIFICATE IN APPLIED INDUSTRIAL ELECTRONICS

YEAR 1 DIGITAL PRINCIPLES

THEORY LESSON 4

Written by Peter Phillips, 1990

BINARY NUMBERS - BINARY ADDITION

OBJECTIVES: At the end of this lesson you should be able to:

(a) *Convert a decimal number (0 to 127) to its binary equivalent.*
(b) *Convert an 8 bit (max) binary number to its decimal equivalent.*
(c) *Perform addition with four bit binary numbers.*
(d) *Draw the circuit of a binary half adder.*
(e) *Show how two half adders can be connected to form a full adder.*
(f) *Show how four full adders can be interconnected to add 2, four bit binary numbers.*

1. INTRODUCTION

The decimal number system is based on a total of 10 characters, 0 through to 9. Other numbering systems that use any number of characters are just as valid as the decimal numbering system, and find application in digital circuits. The three most common systems used are:

(a) The **BINARY** system. Contains 2 characters, 0 and 1. Used in logic circuits, and forms the basis for any form of mathematics when considering a digital logic circuit.

(b) The **OCTAL** system. Contains 8 characters, 0 to 7. Used by computers, and microprocessor based systems.

(c) The **HEXADECIMAL** system. Contains 16 characters, 0 to 9 and A to F. Used in the same applications as the octal system.

In this lesson the binary system is examined, along with techniques in adding binary numbers. As well, the basic logic circuits that perform binary addition are discussed. Following lessons will examine the Hexadecimal and Octal numbering systems as well as subtraction, division and multiplication of binary numbers.

2. THE BINARY SYSTEM

Because digital circuits operate at two levels, the binary system is the only possible number system that can be applied directly to a digital logic circuit. Conversion between binary and decimal numbers is therefore essential to be able to read numerical data within a logic circuit. Because there are only two characters in the binary system, each numerical value must be expressed using a series of 1's and 0's. When a number is written in the decimal system 10 characters are available, and

the characters for numbers greater than 9 are written in a particular order, in which the position of the character within the number identifies its "weighting". Consider the decimal number 4628. In effect, this number is the sum of:

4×10^3, 6×10^2, 2×10^1, and 8×10^0.

That is, 4000 + 600 + 20 + 8, which equals 4628

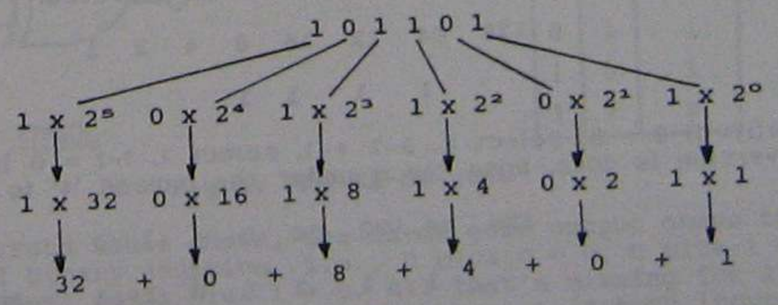
** (note that any number raised to the power of 0 = 1)

This example demonstrates the *weighting* of each digit in that its effect is determined by its *position* within the number. The left-hand digit is the most significant, and the right-hand digit is the least. In a decimal number, each digit is multiplied by a power of 10, because the system is based on the number 10. Thus, "10" is the base, or radix, of the decimal system. In the binary system, the radix is "2", and each digit has a value within the complete number equal to its numerical value (either 0 or 1) multiplied by its weighting. The important values to know are the various powers of two, the first eight of which are listed below.

$2^0 = 1$
$2^1 = 2$
$2^2 = 4$
$2^3 = 8$
$2^4 = 16$
$2^5 = 32$
$2^6 = 64$
$2^7 = 128$

EXAMPLE: BINARY TO DECIMAL
Convert the binary number 101101 to its decimal equivalent.

SOLUTION
(a) Write the binary number as shown, and for each '1' in the number, write the value it represents. Then sum these numbers for the answer.



which equals 45_{10}

Conversion from a decimal value to its binary equivalent can be done in various ways, including successive division/multiplication by 2, a calculator or with the following very simple method:

EXAMPLE: DECIMAL TO BINARY
Convert the decimal number 123 to its binary equivalent.

SOLUTION:
(a) Write the powers of 2 across the top of the page:

128 64 32 16 8 4 2 1

(b) Write a 1 beneath the highest value from this list that when subtracted from the decimal number gives a positive answer. In this example, choose 64 from the list as 128 is too high:

128 64 32 16 8 4 2 1

1

(c) Subtract this value (64) from the decimal number:

123 - 64 = 59

(d) Repeat step (b) using the result of the previous subtraction as the decimal number. Write a 0 beneath unused numbers.

128 64 32 16 8 4 2 1

1 1

(e) Subtract selected value from result of previous subtraction:

59 - 32 = 27

(f) Repeat steps (d) and (e) until the conversion is complete: Thus, next power of two selection is 16: (next less than 27).

128 64 32 16 8 4 2 1

1 1 1

Subtracting: 27 - 16 = 11, allowing 8 to be selected:

128 64 32 16 8 4 2 1

1 1 1 1

Finally: 11-8 = 3, select 2. 3-2 = 1, select 1. 1-1 = 0 indicating conversion is done. Note the 0 under the unused '4' in the list.

128 64 32 16 8 4 2 1

1 1 1 1 0 1 1 = **Answer**

This method is best done by entering the number to be converted on a calculator and keeping a running total as each subtraction is performed. Note that an odd decimal number will always have a 1 as the least significant bit (LSB) in the binary value, and an even decimal number will have 0 as the LSB in the binary value.

The highest decimal number that can be expressed by N binary digits (bits) equals $2^N - 1$. The range of numbers that can be expressed by N bits equals 2^N. *(Teacher note: give more examples of the above).*

3. BINARY ADDITION

Binary numbers are added in the same way as decimal numbers, using the following rules:

```
    0 + 0 = 0
    0 + 1 = 1
    1 + 0 = 1
    1 + 1 = 0 with a carry of 1
1 + 1 + 1 = 1 with a carry of 1
```

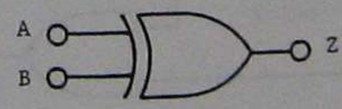
EXAMPLE:

```
  1 1 1 1
  1 0 1 1 +
  \ \ \ \
1 1 0 1 0
```

Analysis: The 1st column produced a carry and a sum of 0. The 2nd column has the sum of 1+1+ carry from column 1, giving a total of 1 and a carry of 1. (Note: 1+1+1 = 3 which in binary equals 11). The 3rd column has the sum of 1 (carry from column 2) +1+0 giving a sum of 0 and a carry of 1. The 4th column has a sum of 1 (carry from column 3) +1+1, giving a sum of 1 and a carry of 1.

4. ADDER CIRCUITS

Binary addition is relatively easy to accomplish. The basic gate used in binary addition is the EX-OR gate and the symbol and truth table are shown in Fig.1 below.



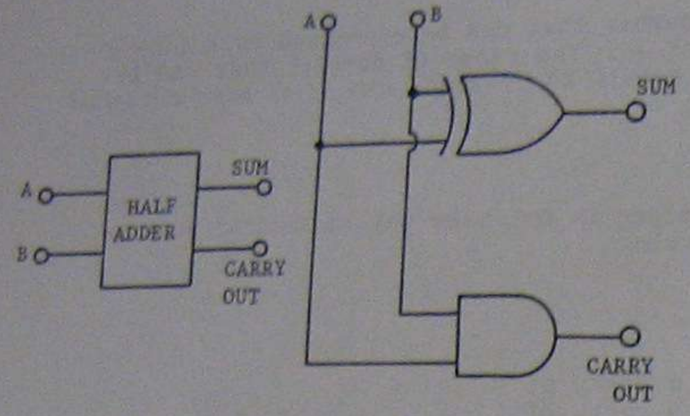
SYMBOL

TRUTH TABLE

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

Fig.1: *The EX-OR gate*

As the truth table shows, the EX-OR gate output obeys the rules of binary addition, i.e., 0 plus 0 = 0, 0 plus 1 = 1, 1 plus 0 = 1 and 1 plus 1 = 0. All that's missing for 1 plus 1 is the carry. The gate that outputs a 1 if both inputs are 1 is the AND gate. Thus, by connecting an AND gate in parallel with the EX-OR gate, a circuit capable of adding two binary bits can be realised. This circuit is called a half adder, shown along with its truth table in Fig.2.



TRUTH TABLE

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig.2: The Half Adder

The half adder is only able to add two binary bits and doesn't allow for a carry in from a previous addition. By combining two half adders and ORing the Carry Out terminals from both, the *Full Adder* is constructed. The sum out of one half adder feeds one input of the other half adder, giving a total of three inputs as shown in Fig.3. The truth table for the Full Adder is shown in Fig.4.

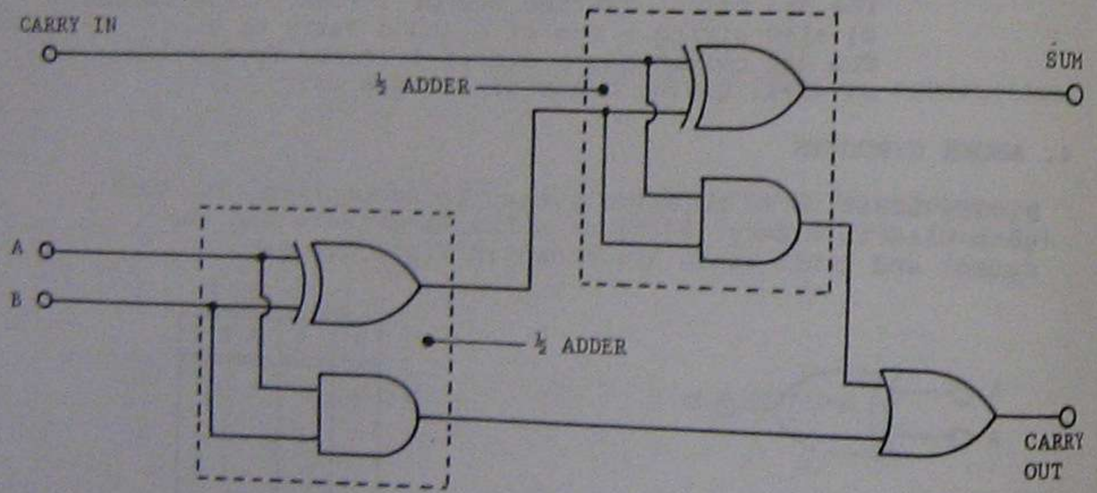


Fig.3(a): *The Full Adder*

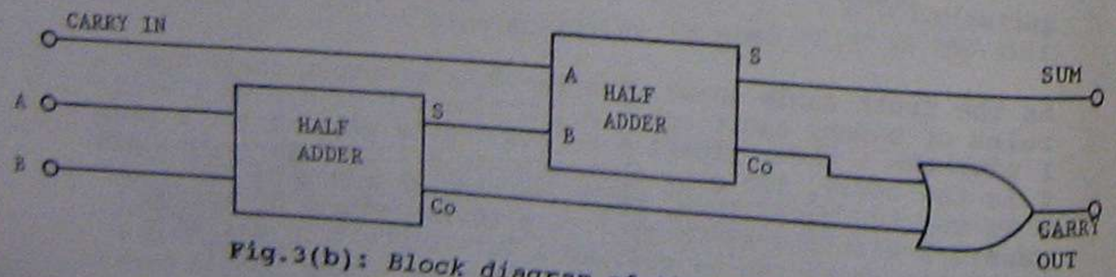


Fig.3(b): *Block diagram of the Full Adder*

INPUTS			OUTPUTS	
A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table for the Full Adder

Combining full adders to allow the addition of two, 4 bit binary numbers requires four full adders to be cascaded, as shown in Fig.5. The first Carry In terminal is set to a logic 0 by grounding it, and each Carry Out terminal connects to the next full adder's Carry In terminal. The 74LS83 is a four bit full adder IC used in binary addition.

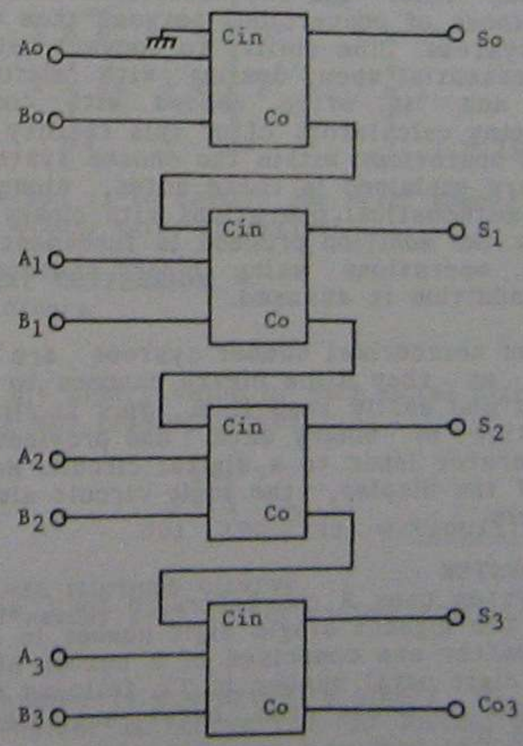


Fig.5: *Cascading 4 full adders to add two, 4 bit binary numbers*